Glenside

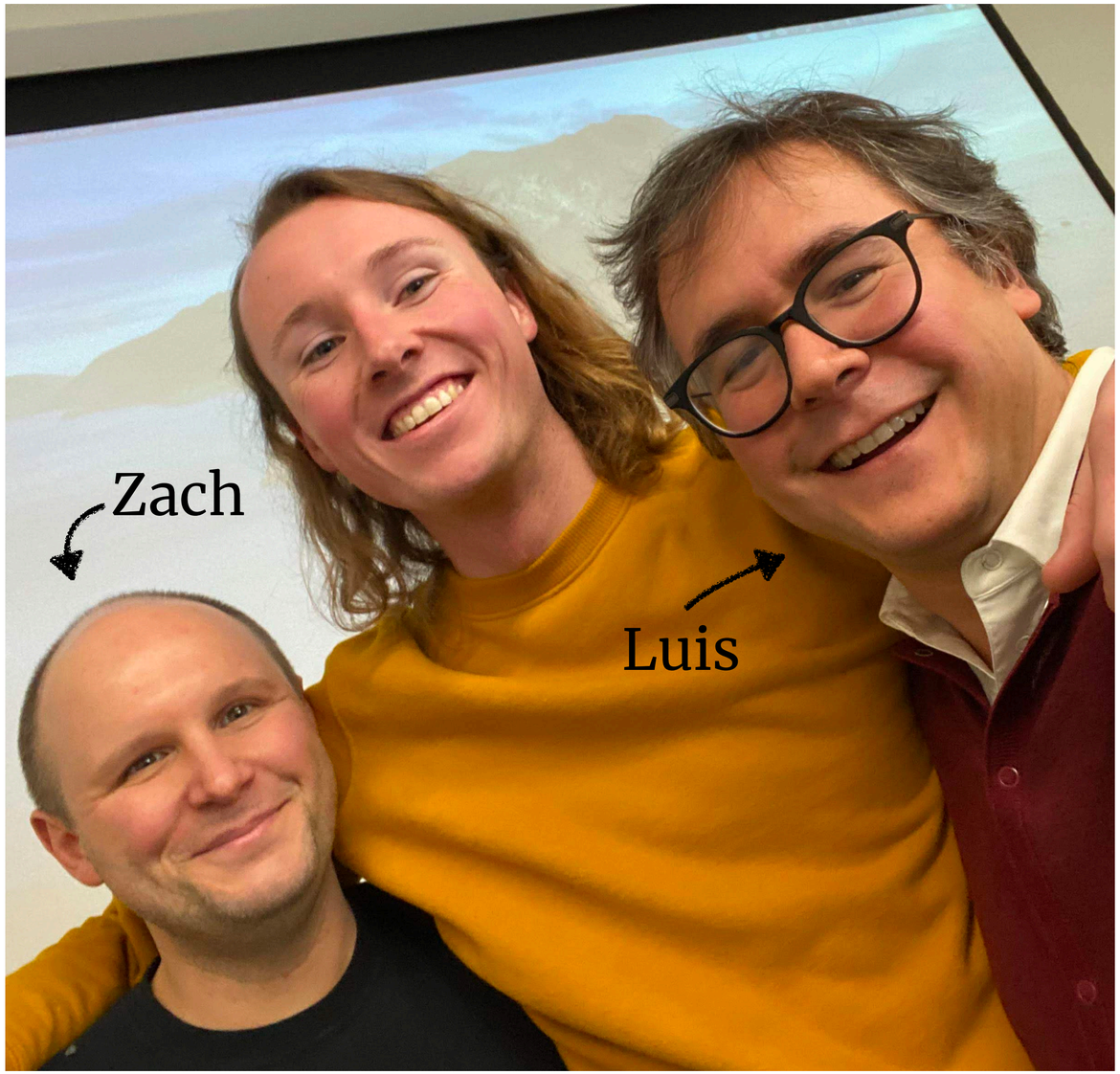
Partitioning Deep Learning Hardware and Software

Gus Smith, University of Washington

PL/Arch External Talk Series @ CAPRA, May 27th, 2020

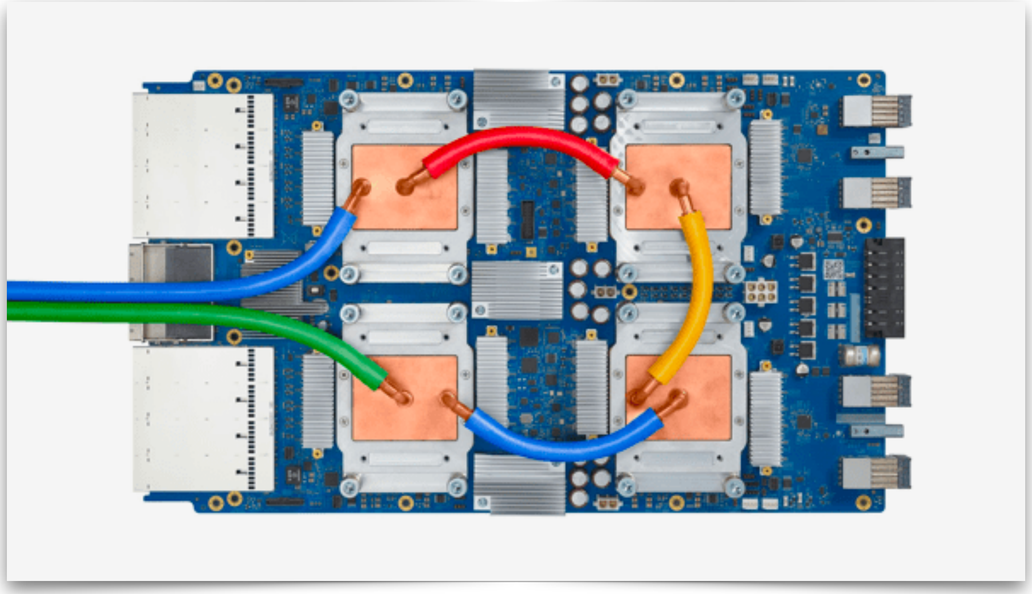
Who?

- 2nd year at UW working in PL/ Arch with Zach Tatlock/Luis Ceze
- Interested in how we can advance architecture w/ PL techniques

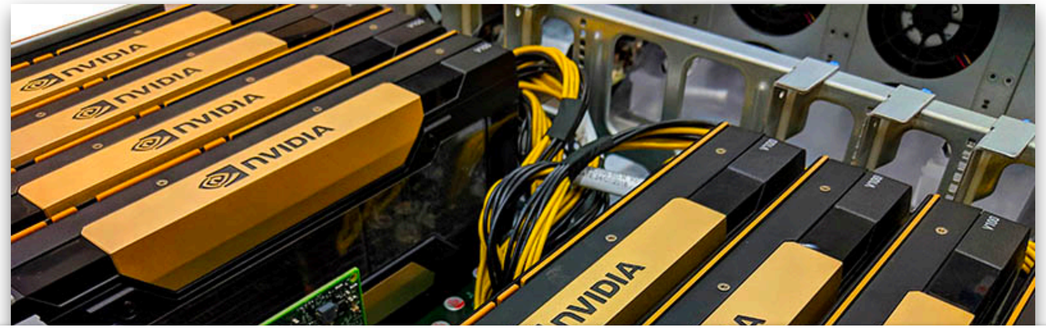


⚠ WIP ⚠

Architects accelerate deep learning with custom hardware.



Architects accelerate deep learning with custom hardware.



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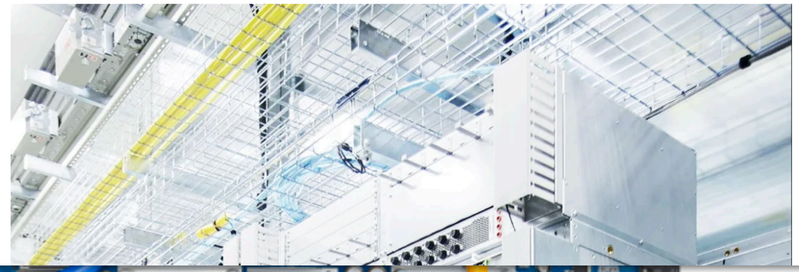
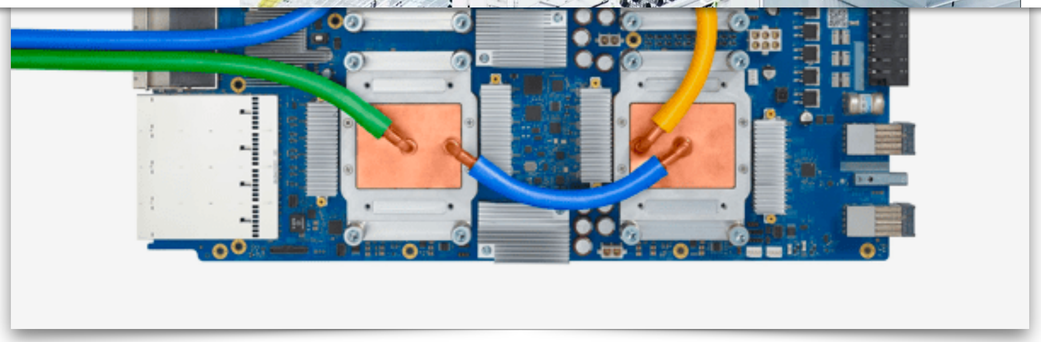
WIRED

Building an AI Chip Saved Google From Building a Dozen New Data Centers





...but designing deep learning stacks is complex!

In-Datacenter Performance Analysis of a Tensor Processing Unit™

Norman P. Jouppi, Cliff Young, Nishant Patil, David Patterson, Gaurav Agrawal, Raminder Bajwa, Sarah Bates, Suresh Bhatia, Nan Boden, Al Borchers, Rick Boyle, Pierre-luc Cantin, Clifford Chao, Chris Clark, Jeremy Coriell, Mike Daley, Matt Dau, Jeffrey Dean, Ben Gelb, Tara Vazir Ghaemmaghami, Rajendra Gottipati, William Gulland, Robert Hagmann, C. Richard Ho, Doug Hogberg, John Hu, Robert Hundt, Dan Hurt, Julian Ibarz, Aaron Jaffey, Alek Jaworski, Alexander Kaplan, Harshit Khaitan, Daniel Killebrew, Andy Koch, Naveen Kumar, Steve Lacy, James Laudon, James Law, Diemthu Le, Chris Leary, Zhuyuan Liu, Kyle Lucke, Alan Lundin, Gordon MacKean, Adriana Maggiore, Maire Mahony, Kieran Miller, Rahul Nagarajan, Ravi Narayanaswami, Ray Ni, Kathy Nix, Thomas Norrie, Mark Omernick, Narayana Penukonda, Andy Phelps, Jonathan Ross, Matt Ross, Amir Salek, Emad Samadiani, Chris Severn, Gregory Sizikov, Matthew Snelham, Jed Souter, Dan Steinberg, Andy Swing, Mercedes Tan, Gregory Thorson, Bo Tian, Horia Toma, Erick Tuttle, Vijay Vasudevan, Richard Walter, Walter Wang, Eric Wilcox, and Doe Hyun Yoon

Google, Inc., Mountain View, CA USA

Email: {jouppi, cliffy, nishantpatil, davidpatterson}@google.com

To appear at the 44th International Symposium on Computer Architecture (ISCA), Toronto, Canada, June 26, 2017.

TensorFlow:
Large-Scale Machine Learning on Heterogeneous Distributed Systems

(Preliminary White Paper, November 9, 2015)

Martín Abadi, Ashish Agarwal, Paul Barham, Eugene Brevdo, Zhifeng Chen, Craig Citro,
Greg S. Corrado, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Ian Goodfellow,
Andrew Harp, Geoffrey Irving, Michael Isard, Yangqing Jia, Rafal Jozefowicz, Lukasz Kaiser,
Manjunath Kudlur, Josh Levenberg, Dan Mané, Rajat Monga, Sherry Moore, Derek Murray,
Chris Olah, Mike Schuster, Jonathon Shlens, Benoit Steiner, Ilya Sutskever, Kunal Talwar,
Paul Tucker, Vincent Vanhoucke, Vijay Vasudevan, Fernanda Viégas, Oriol Vinyals,
Pete Warden, Martin Wattenberg, Martin Wicke, Yuan Yu, and Xiaoqiang Zheng
Google Research*

An Oversimplified View of HW–SW stack design

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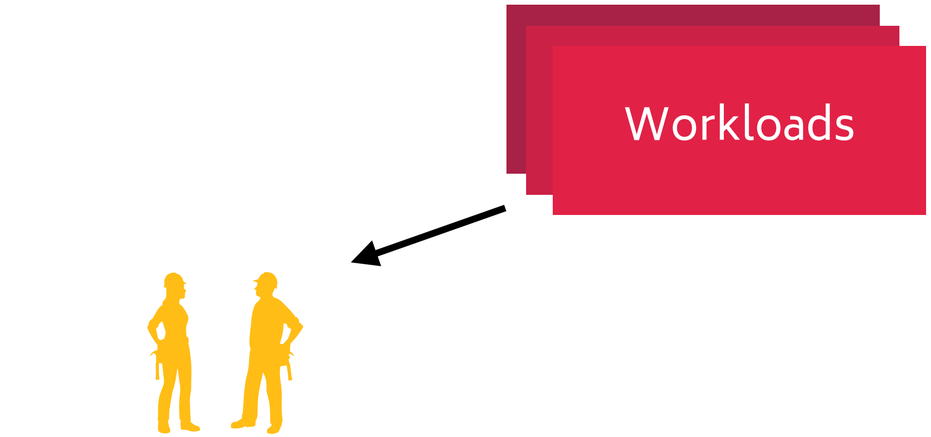

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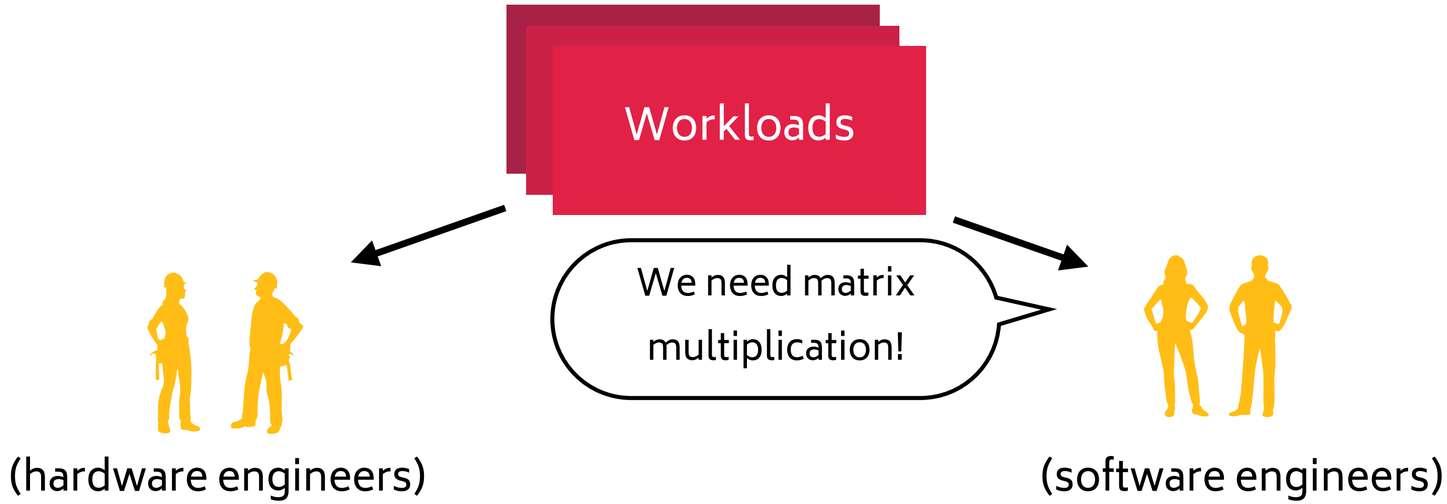

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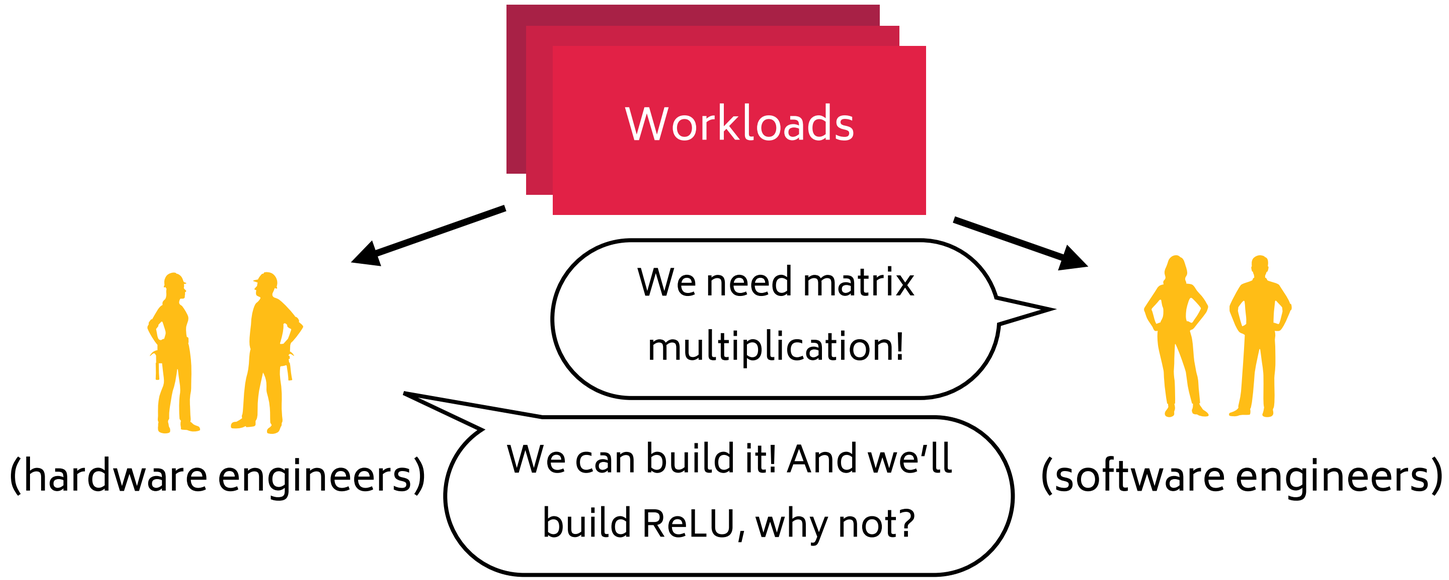

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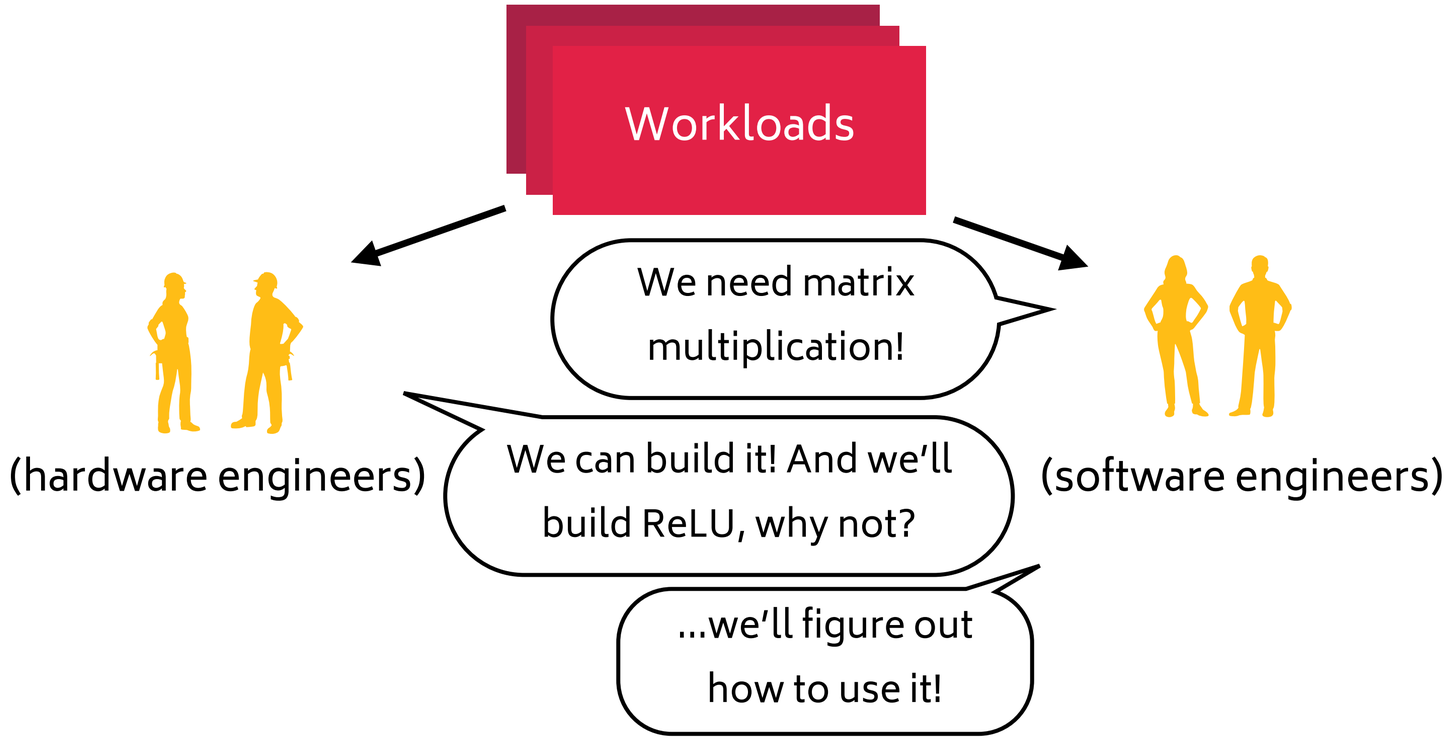

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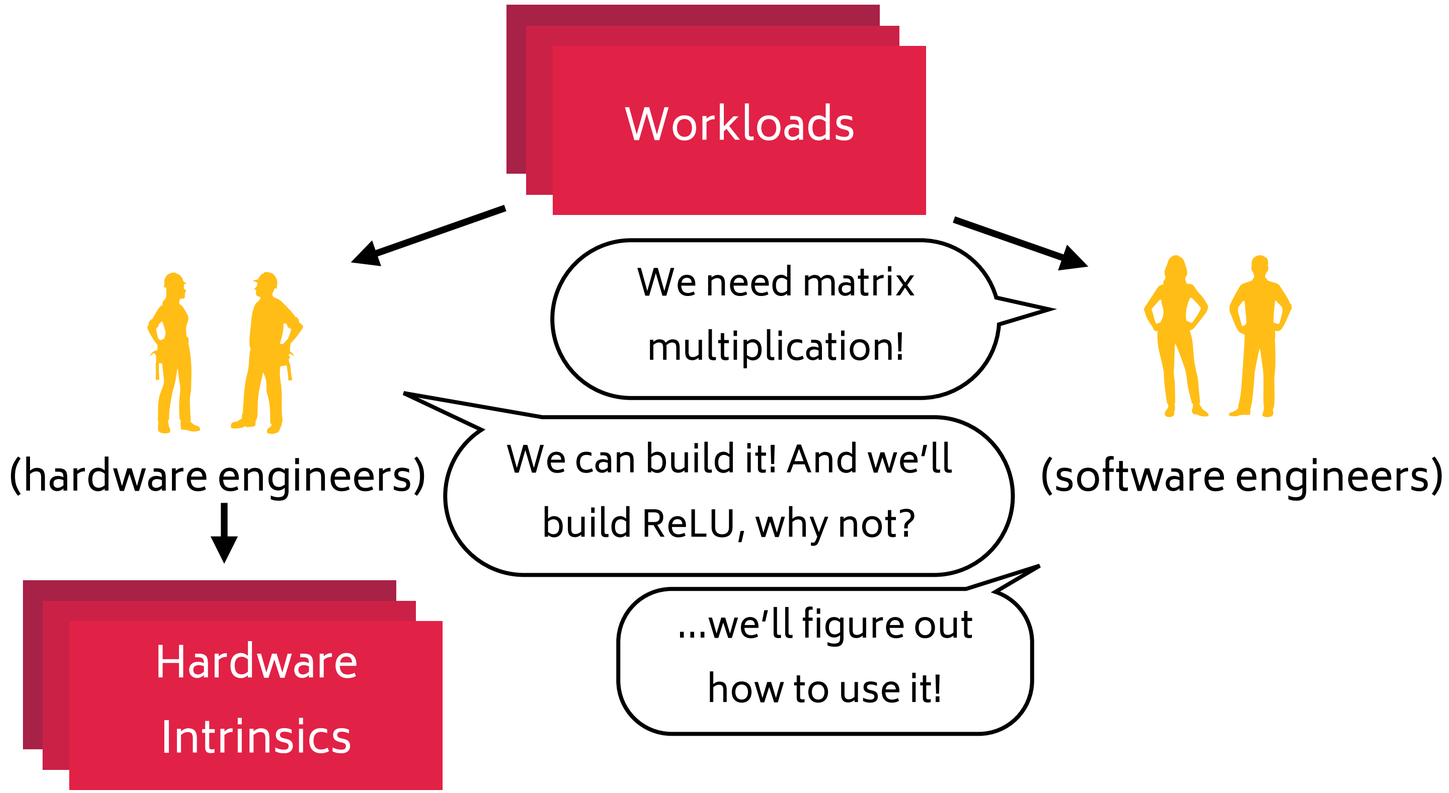

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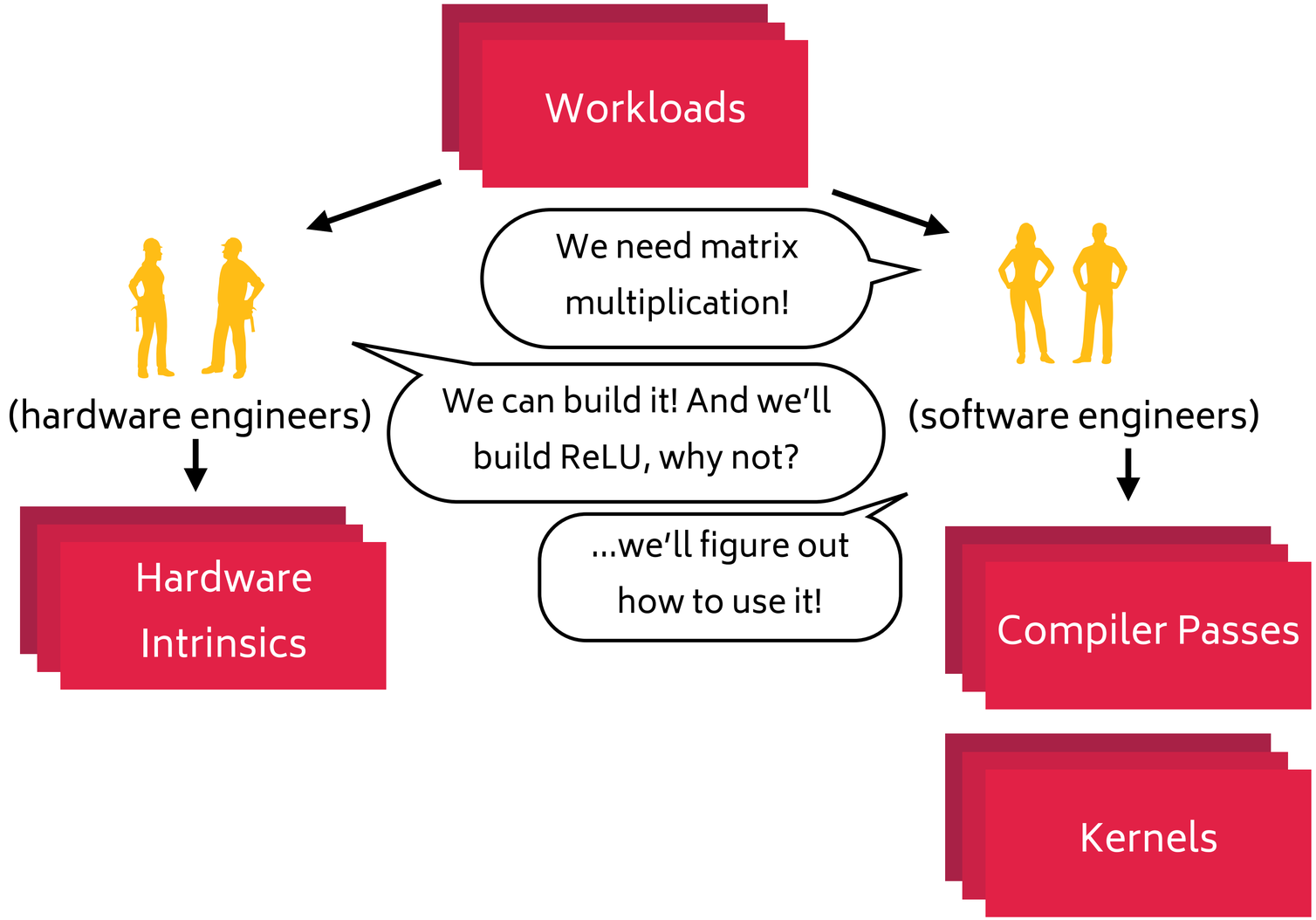

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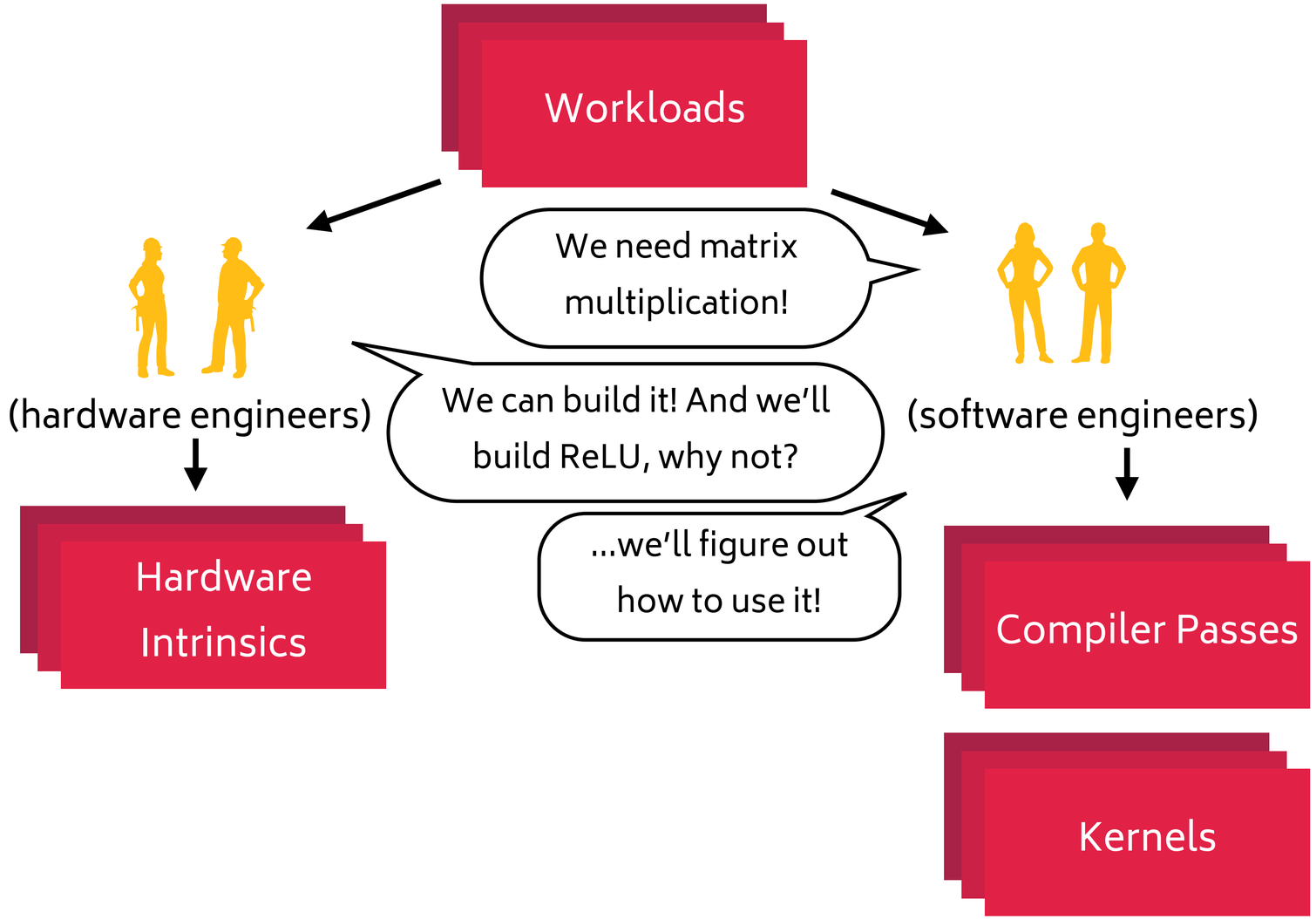

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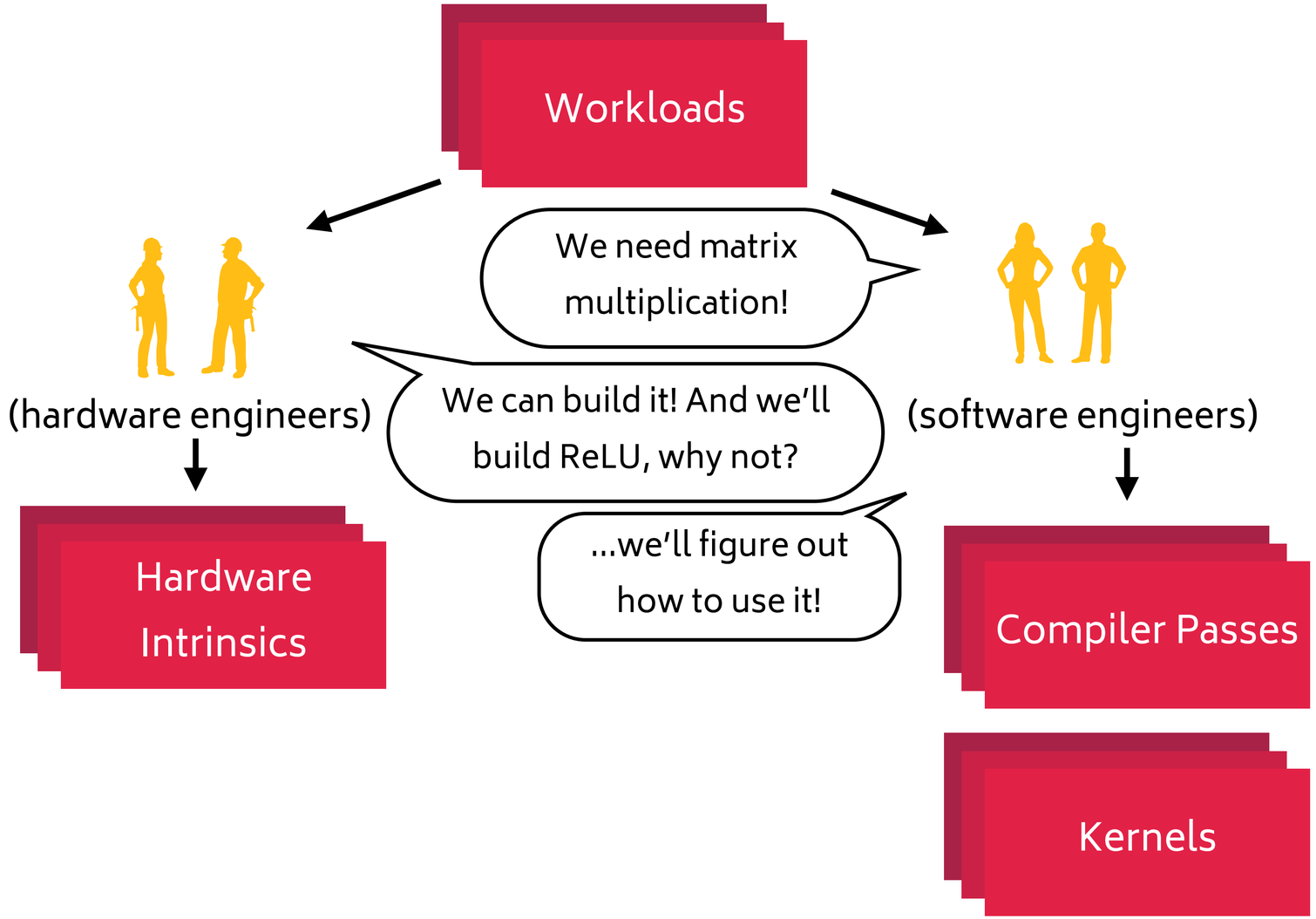

This system makes sense because chips and compilers are massive projects.

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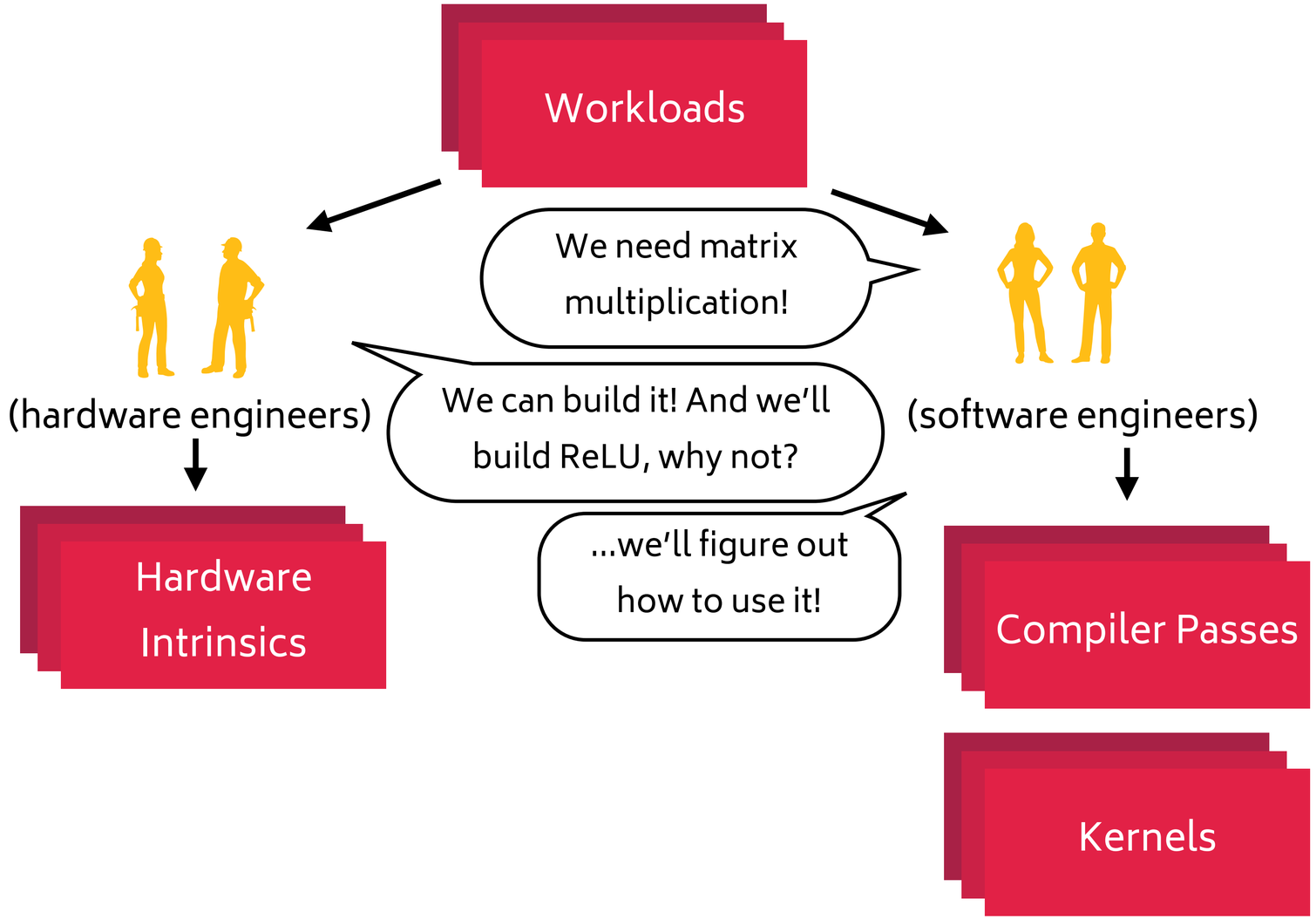

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...but we can't help but notice the inefficiencies!

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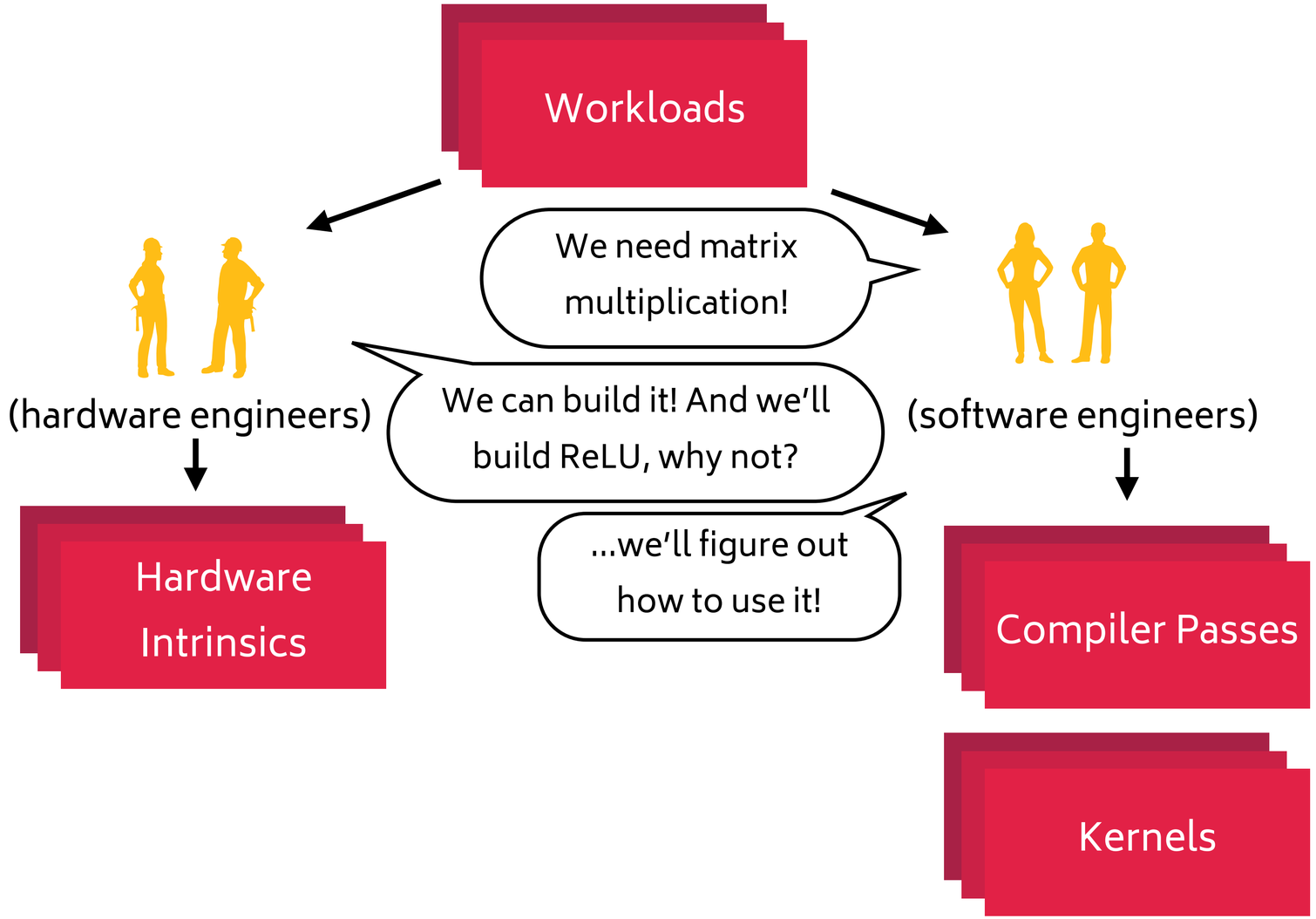

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- Slow

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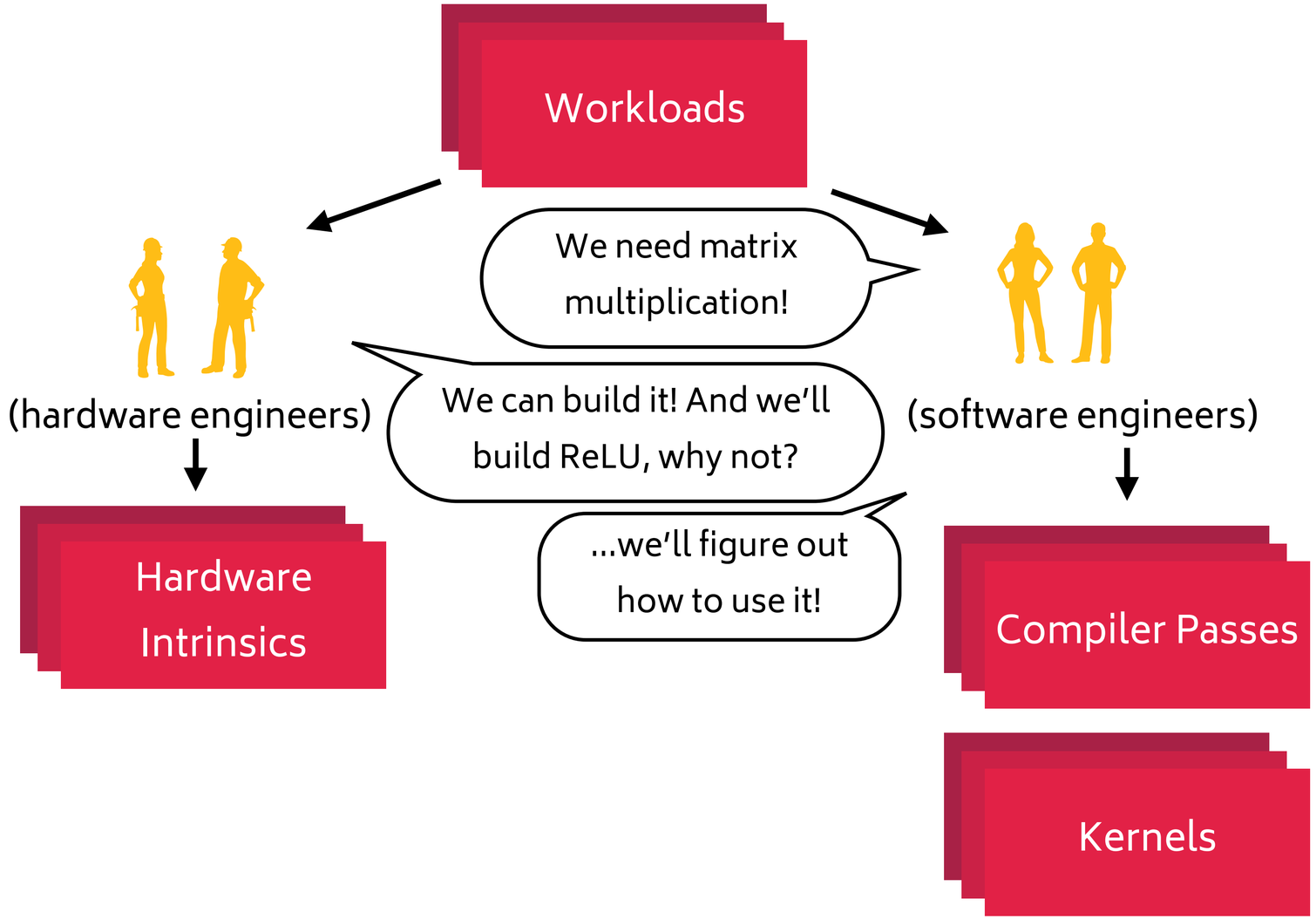

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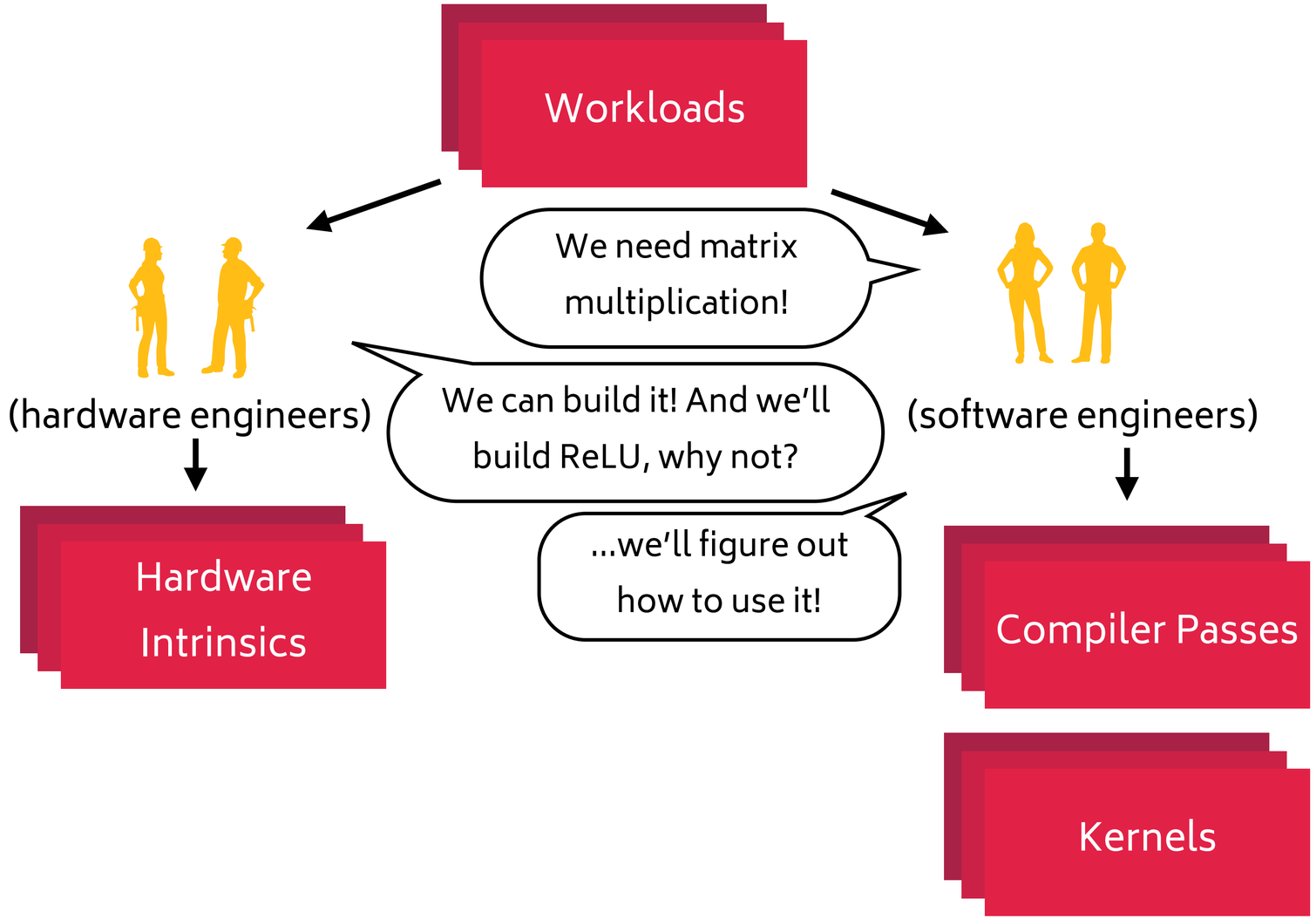

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- Slow
- Misses design points
- Design knowledge is lost in communication!

Why not design the hardware and software at the same time?

A Hardware–Software Codesign Approach

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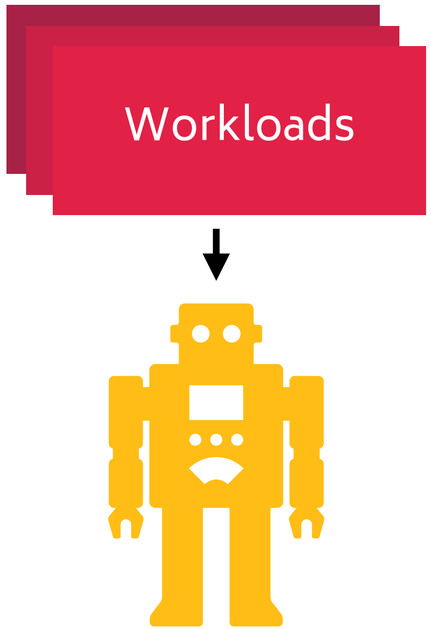

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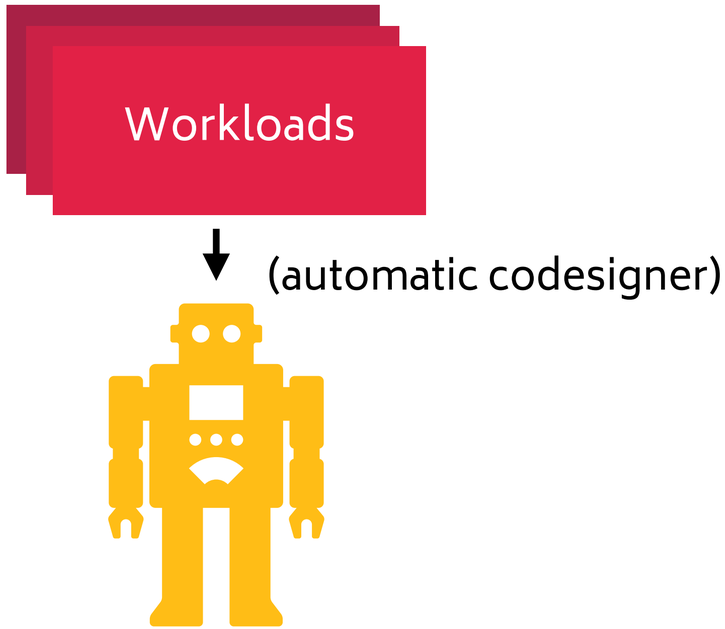

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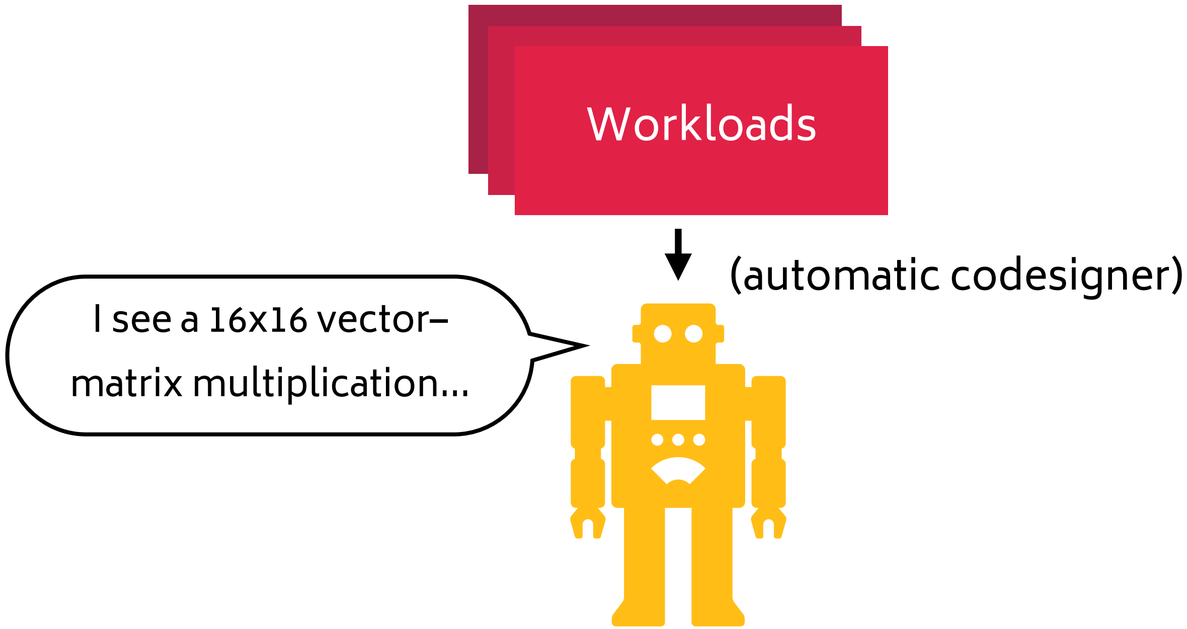

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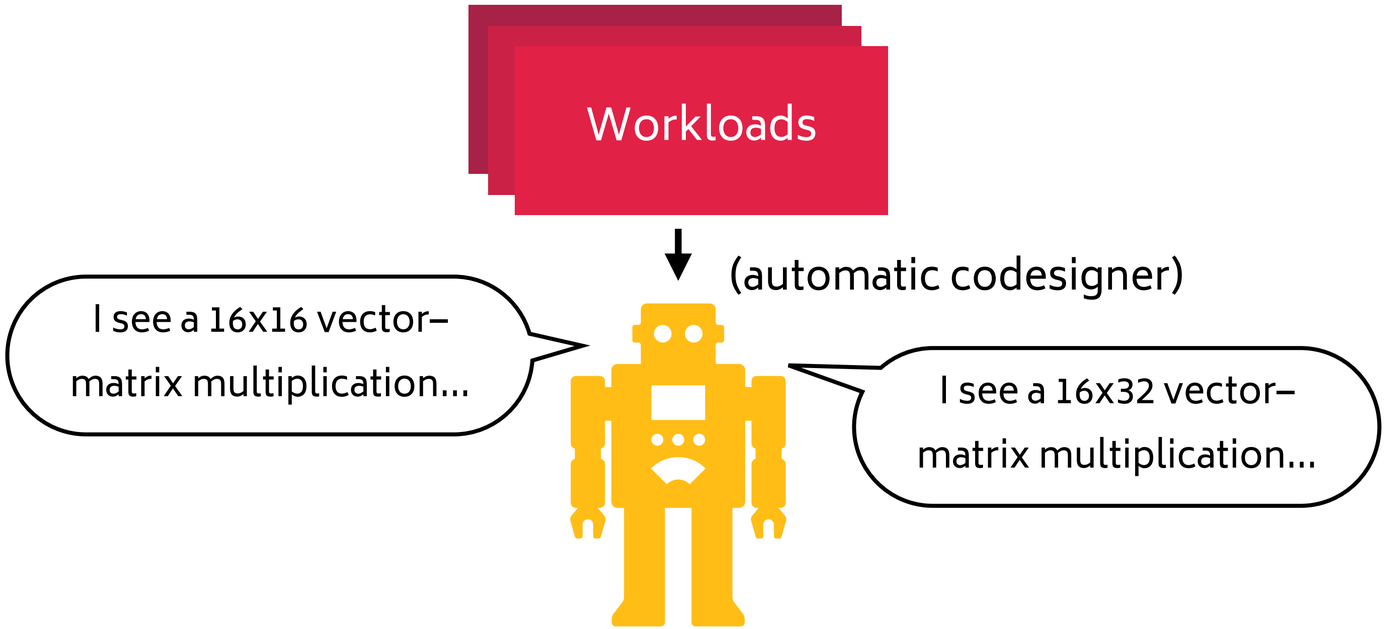

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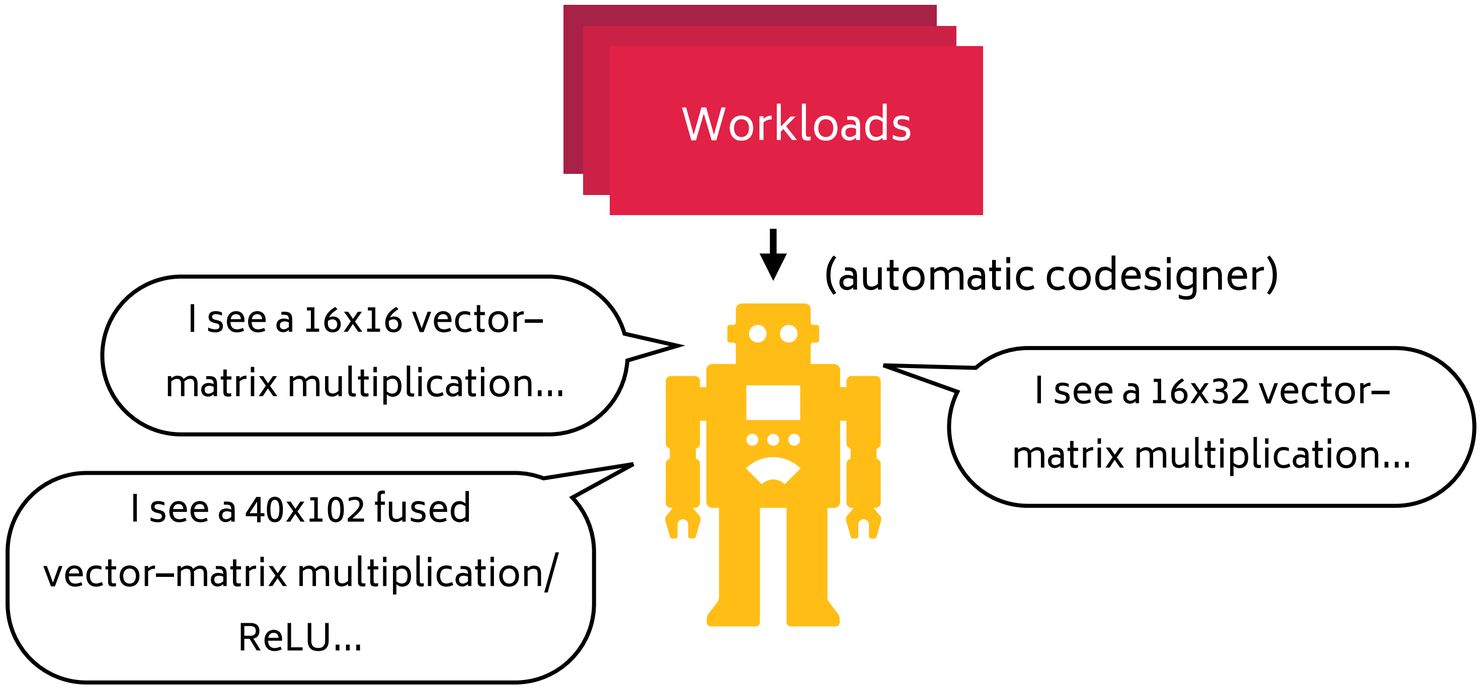

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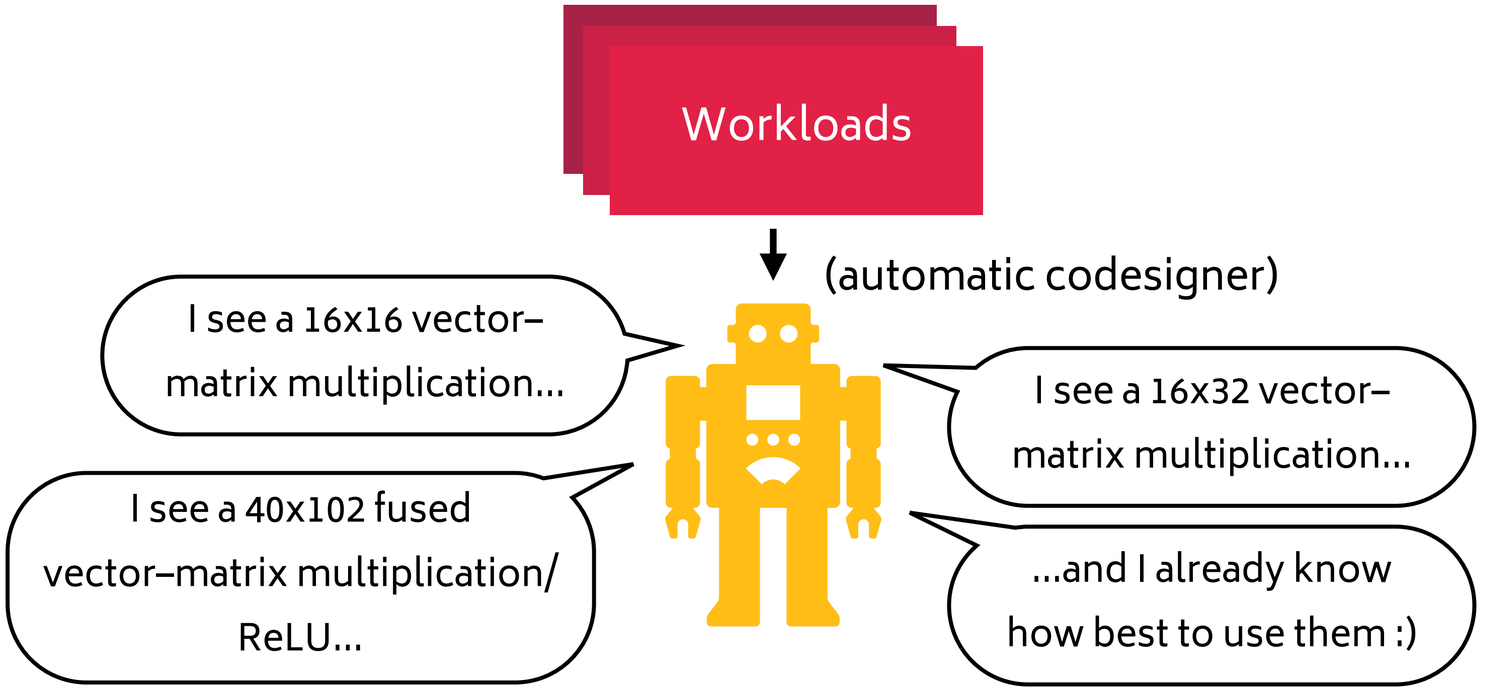

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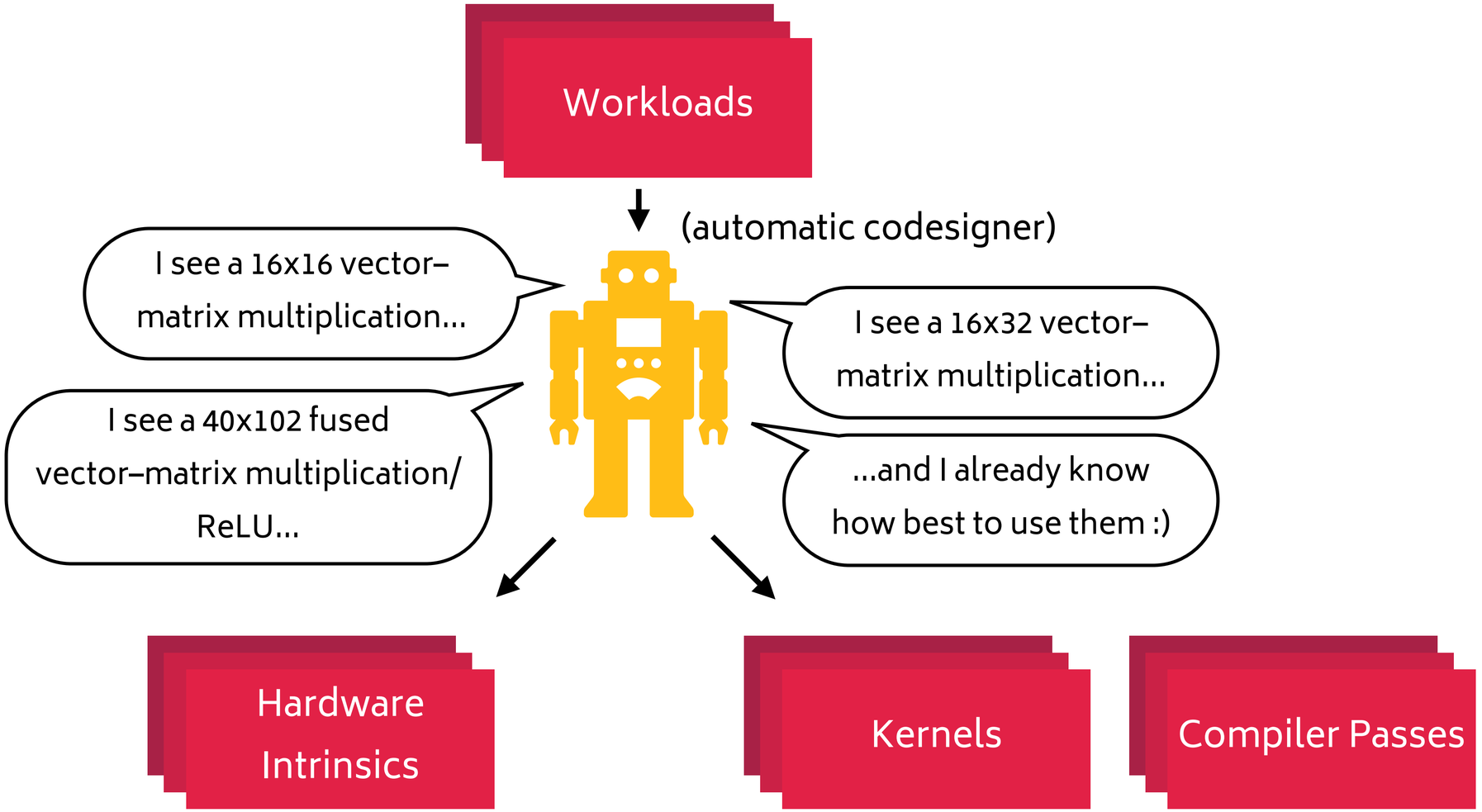

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Hardware–software codesign often raises a healthy amount of skepticism due to its meager success in the past.

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Hardware–software codesign often raises a healthy amount of skepticism due to its meager success in the past.

One of the primary issues is that **the space of potential hardware–software designs is massive!**

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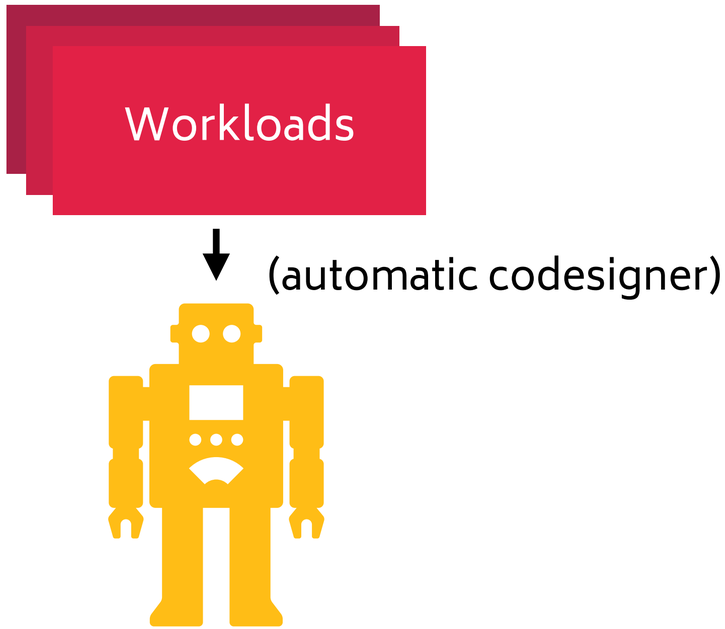

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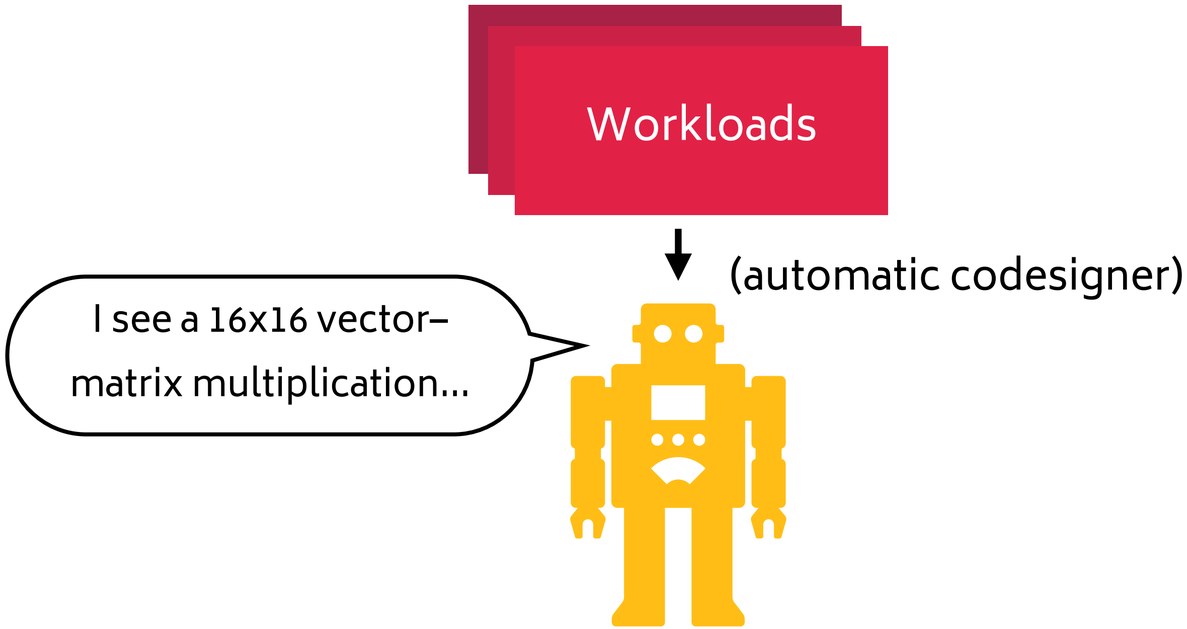

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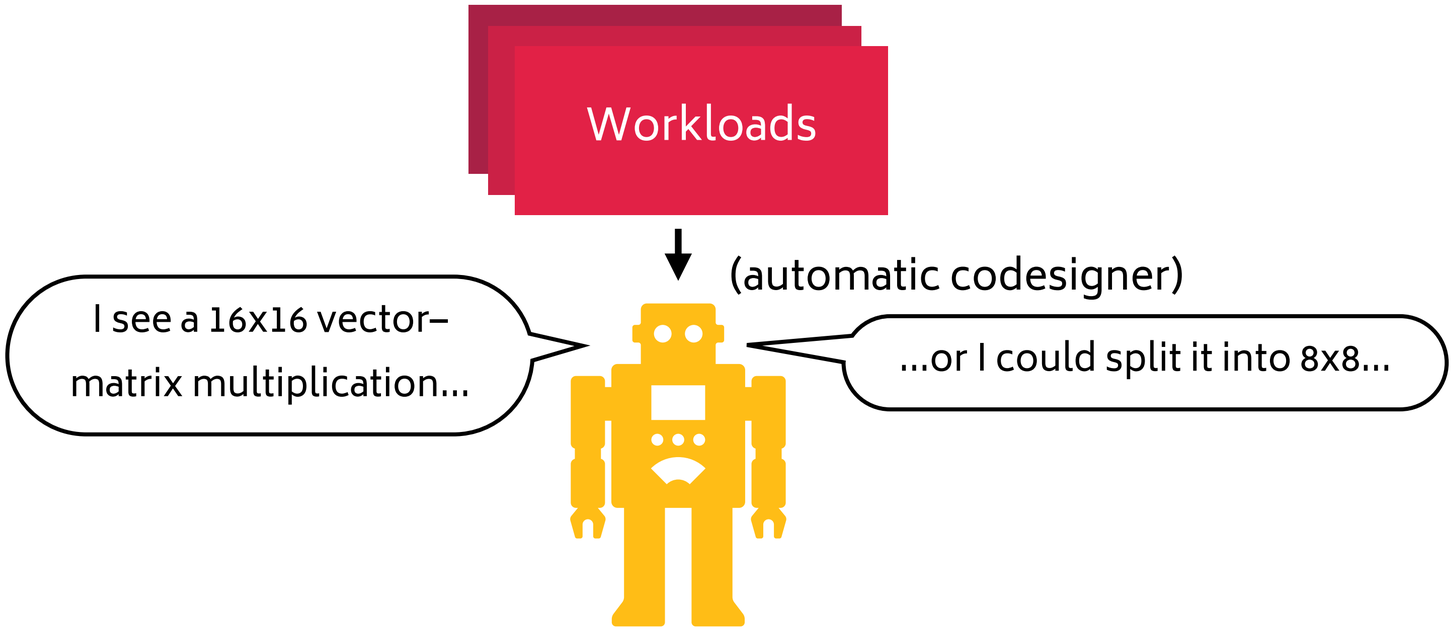

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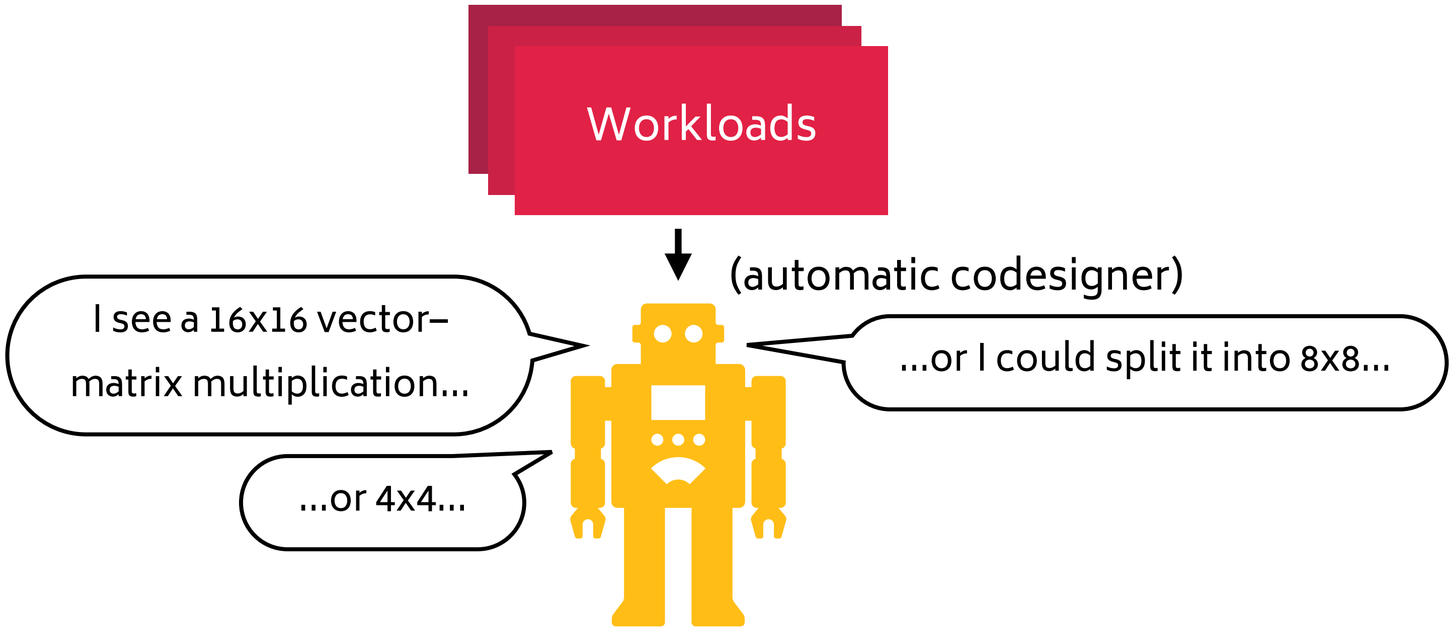

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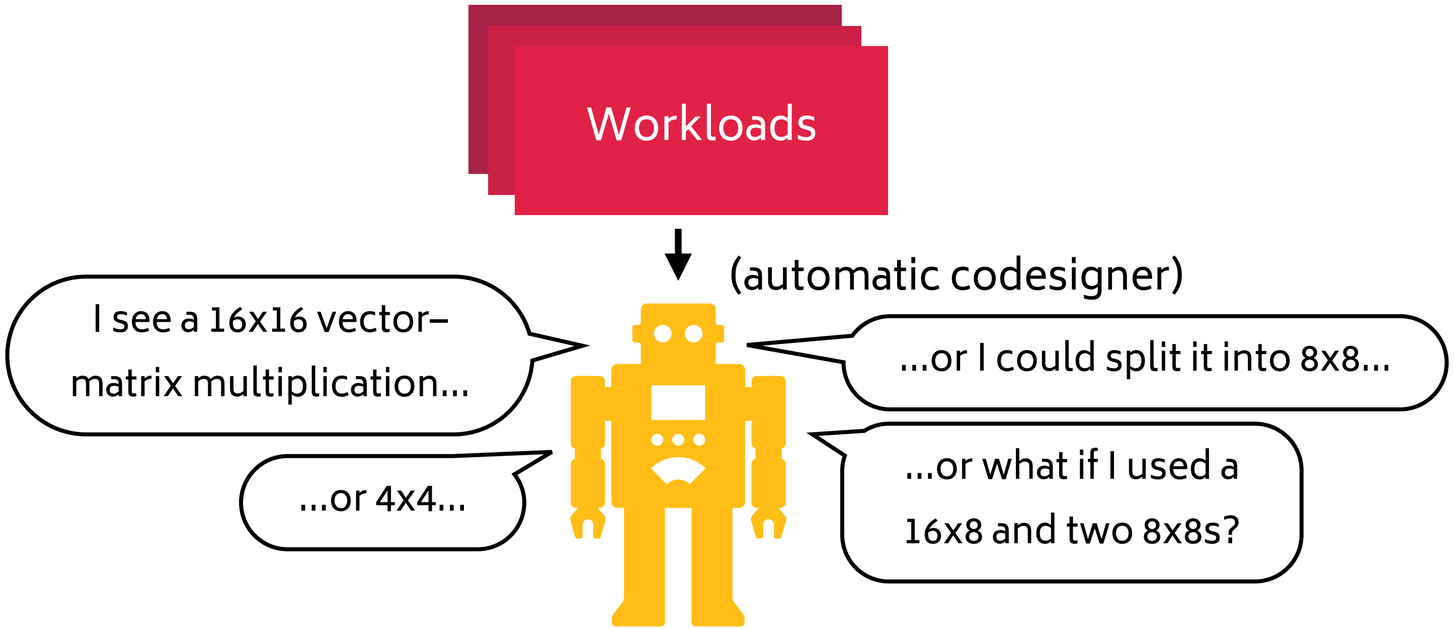

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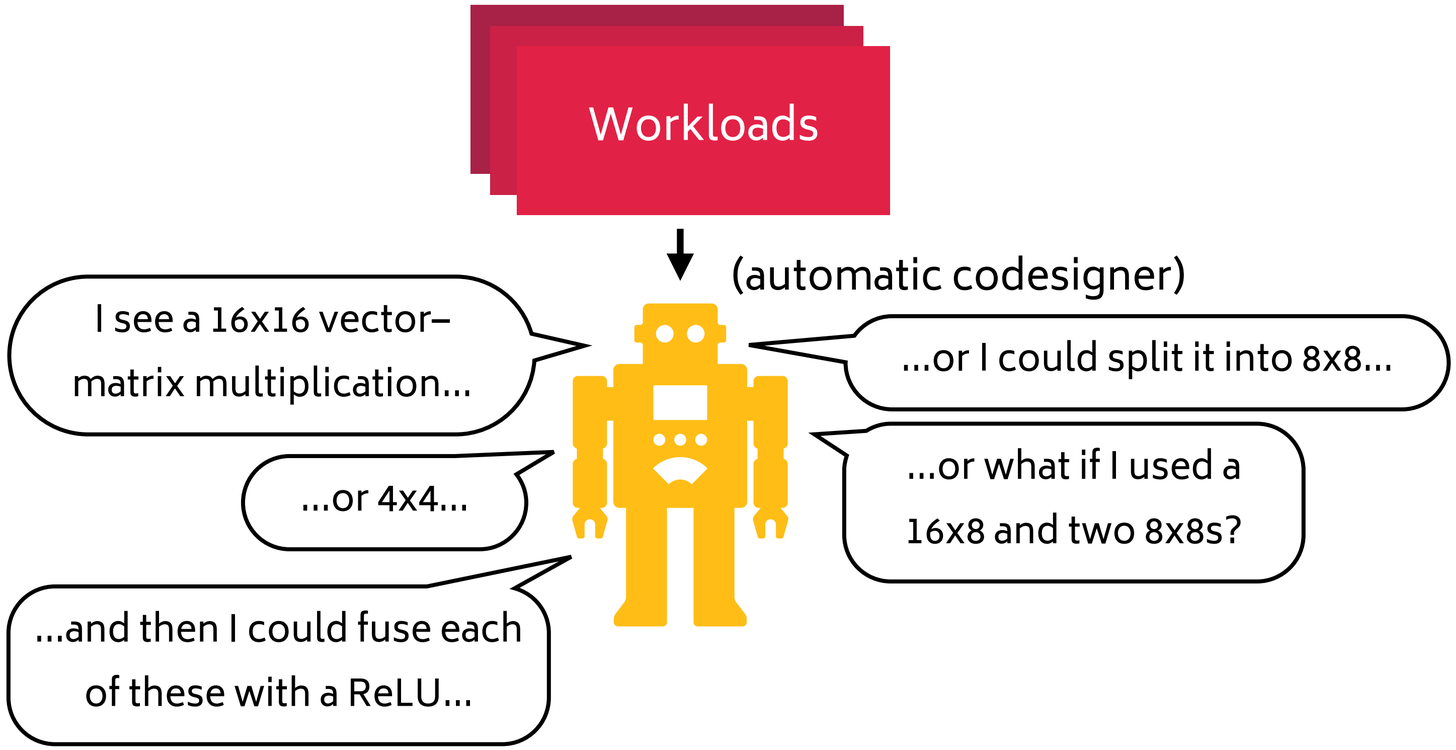

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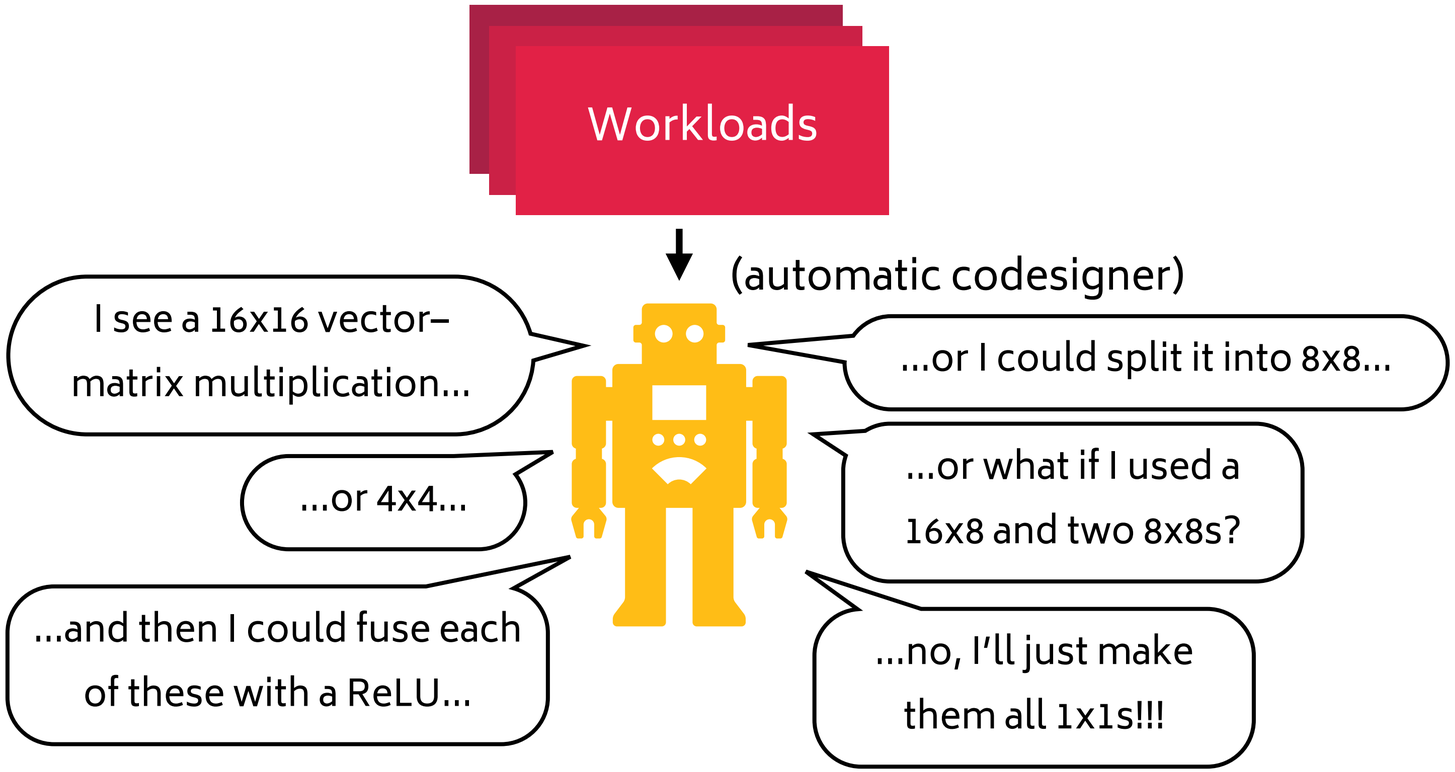

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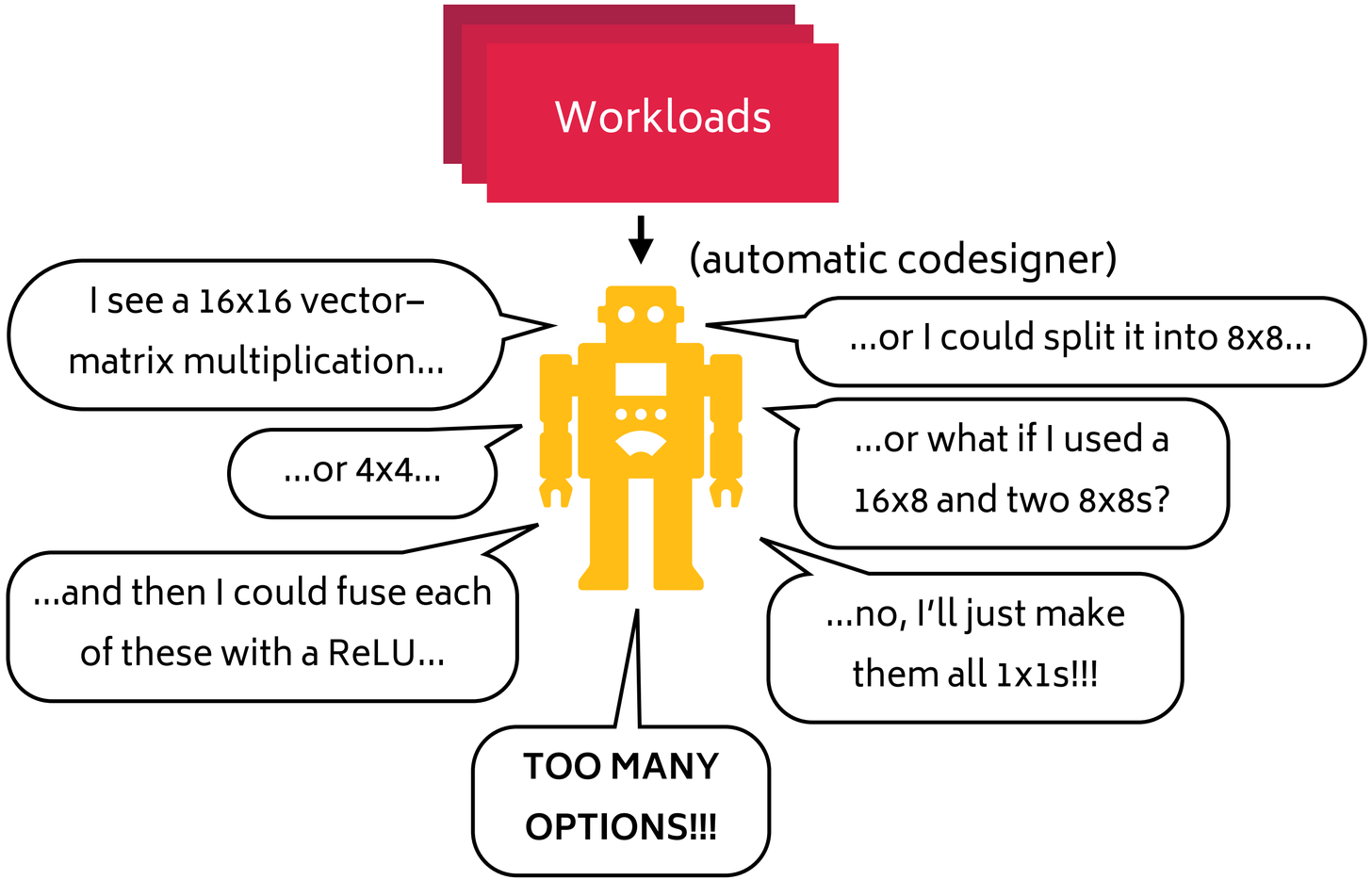

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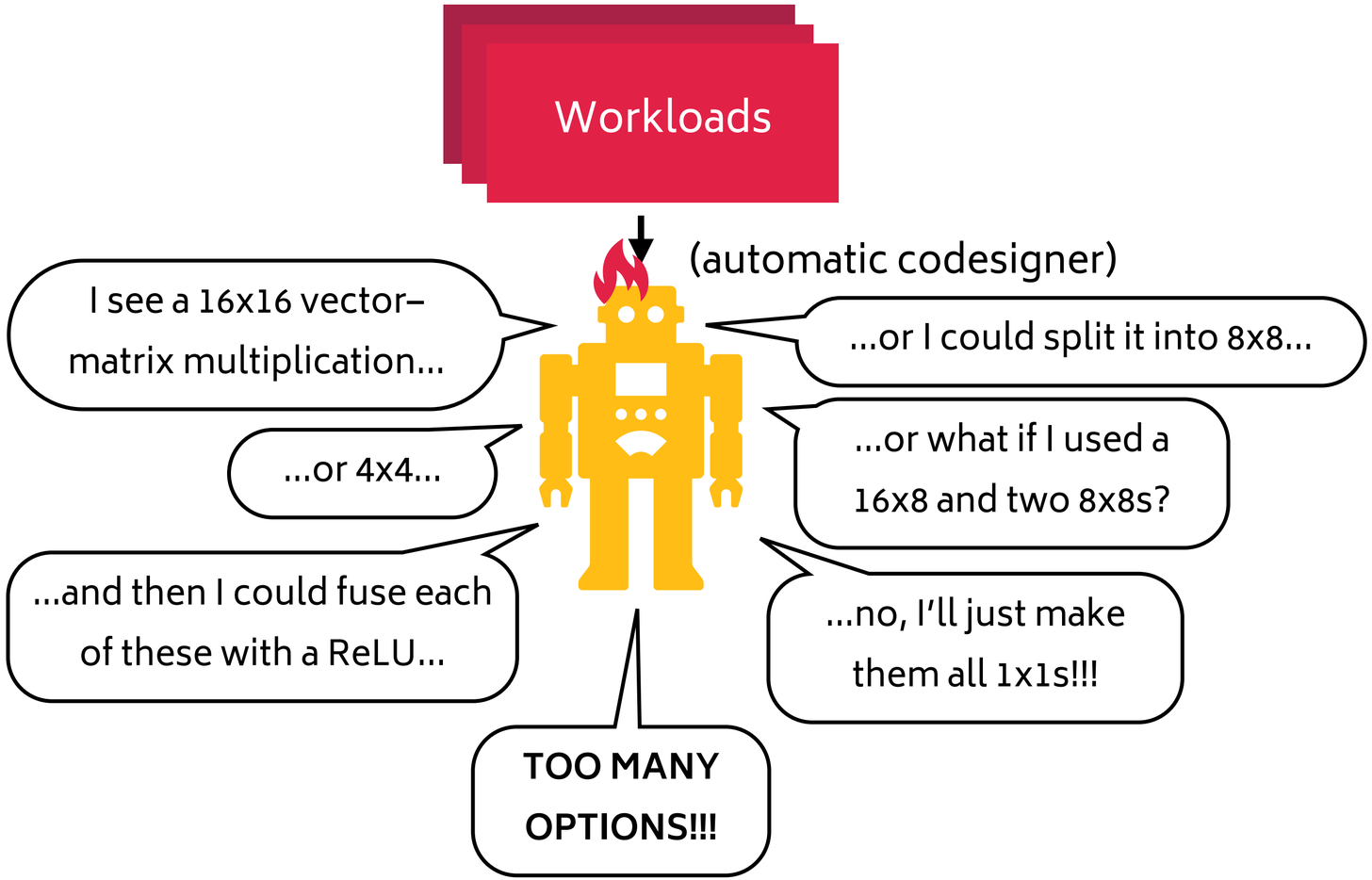

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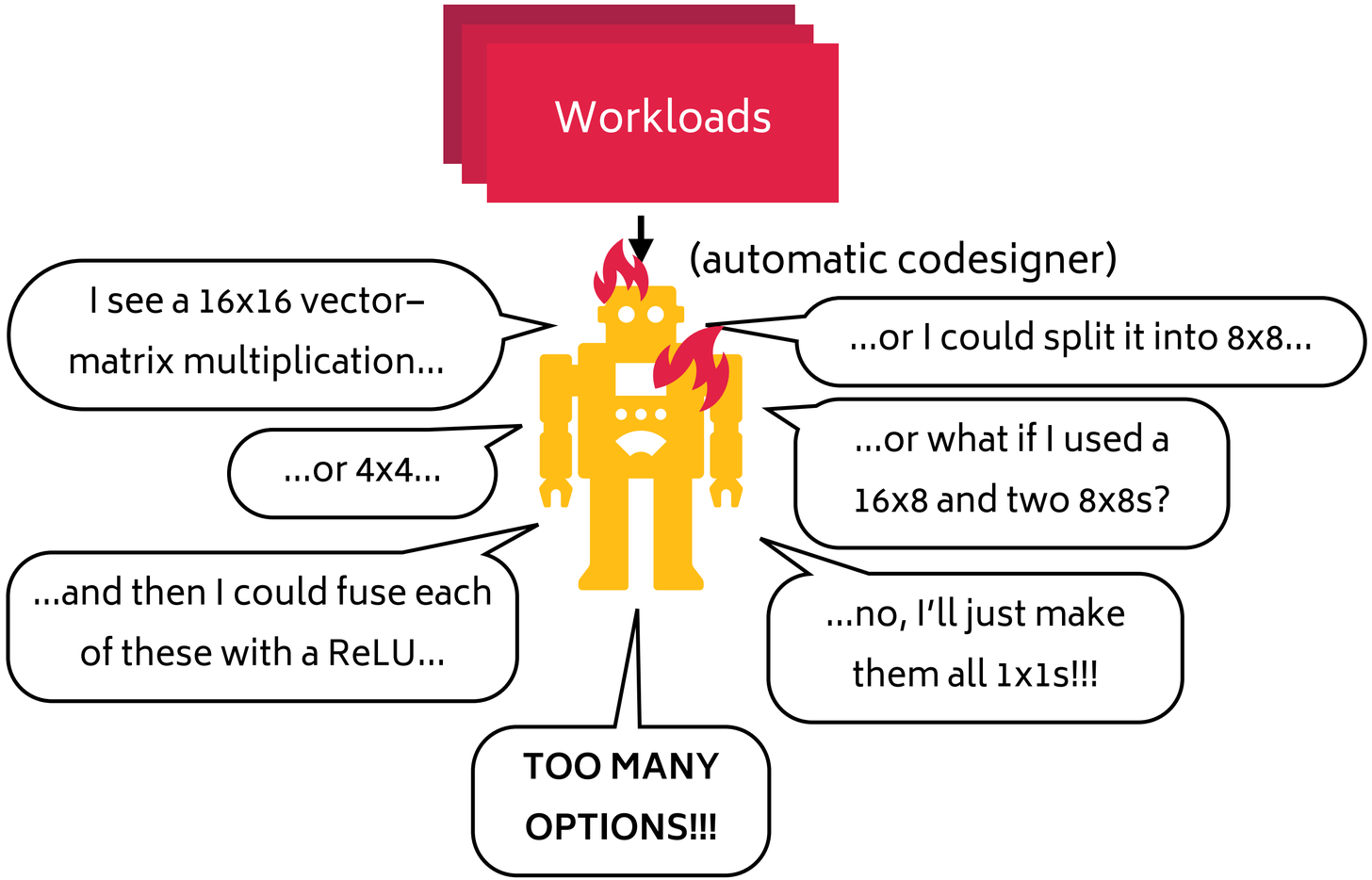

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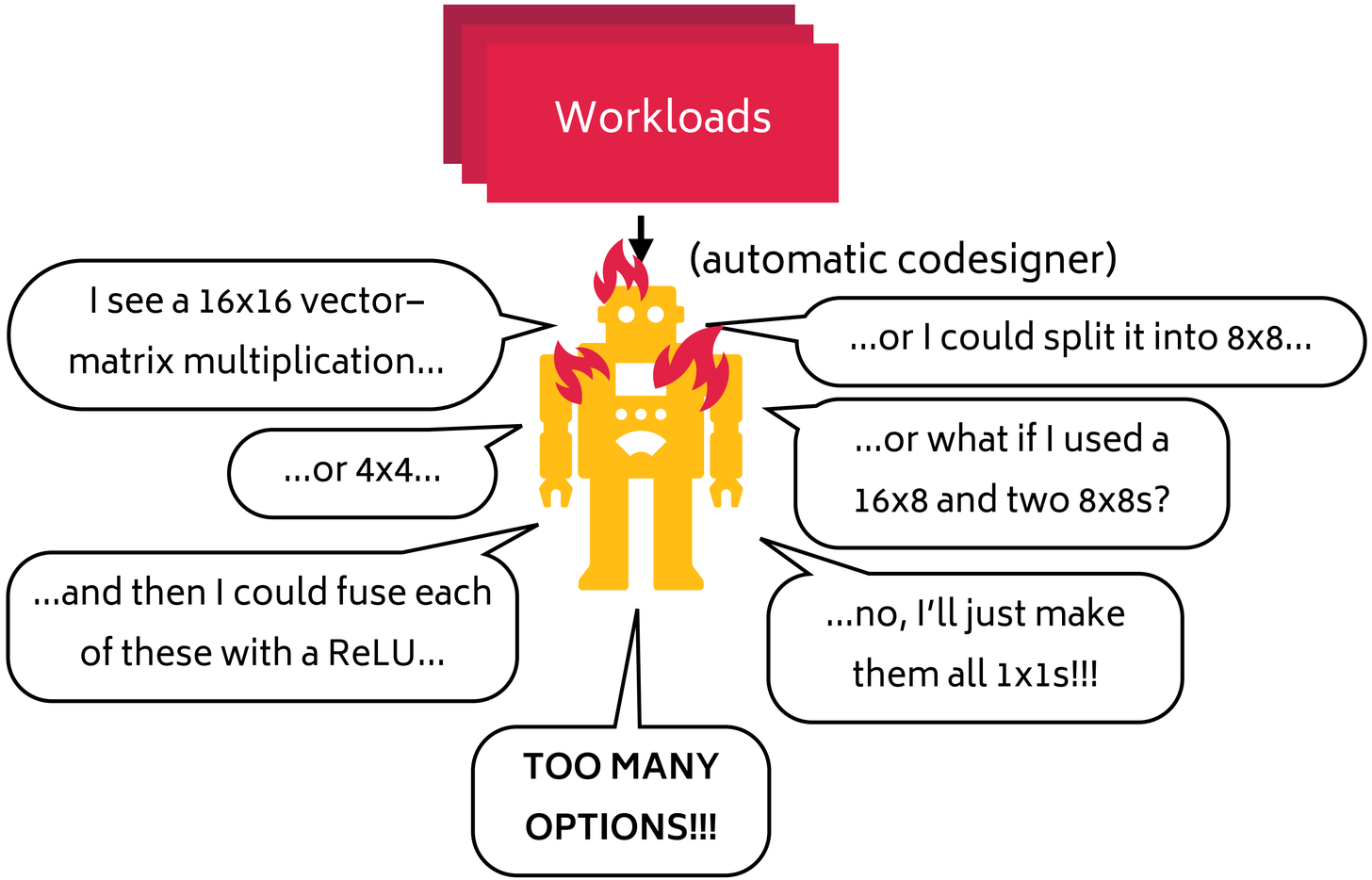
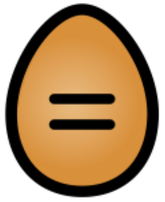


If only we had a tool for representing massive search spaces!



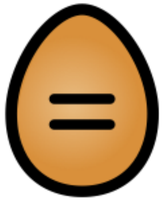
Using E-Graphs for Optimization with egg

Max Willsey

github.com/mwillsey/egg

Remy Wang Chandrakana Nandi Oliver Flatt

Pavel Panchekha Zach Tatlock



Rewriting

$(a*2)/2$

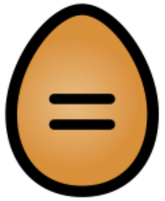
$x*2 \rightarrow x<<1$

$((x*y)*z) \rightarrow (x*(y*z))$

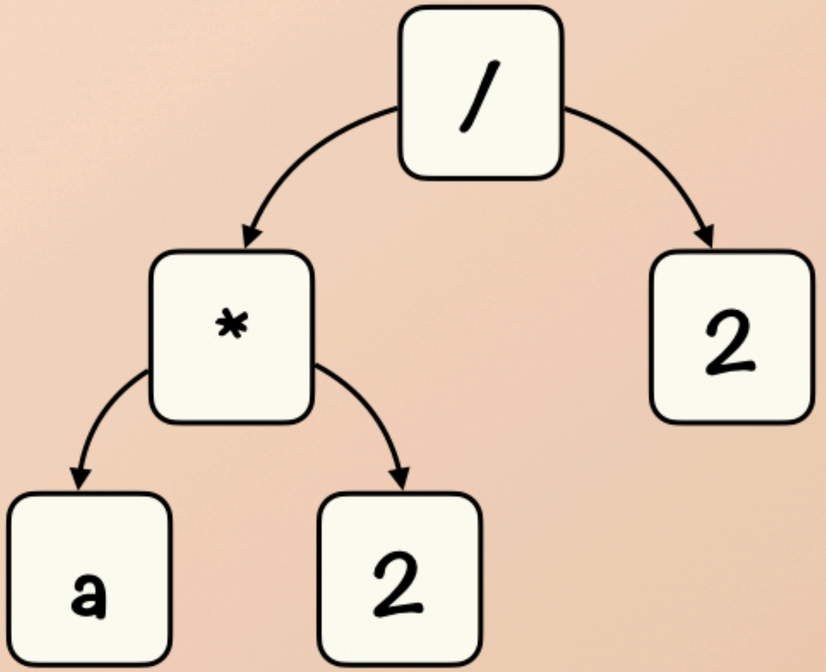
$x/x \rightarrow 1$

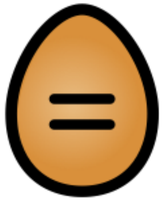
$x*1 \rightarrow x$

$x*y \rightarrow y*x$



Term Graphs





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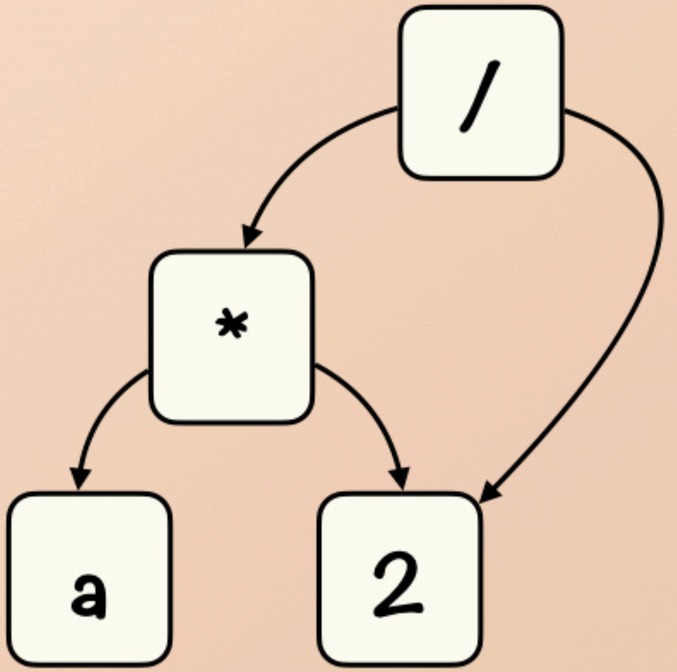
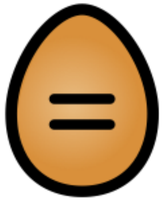
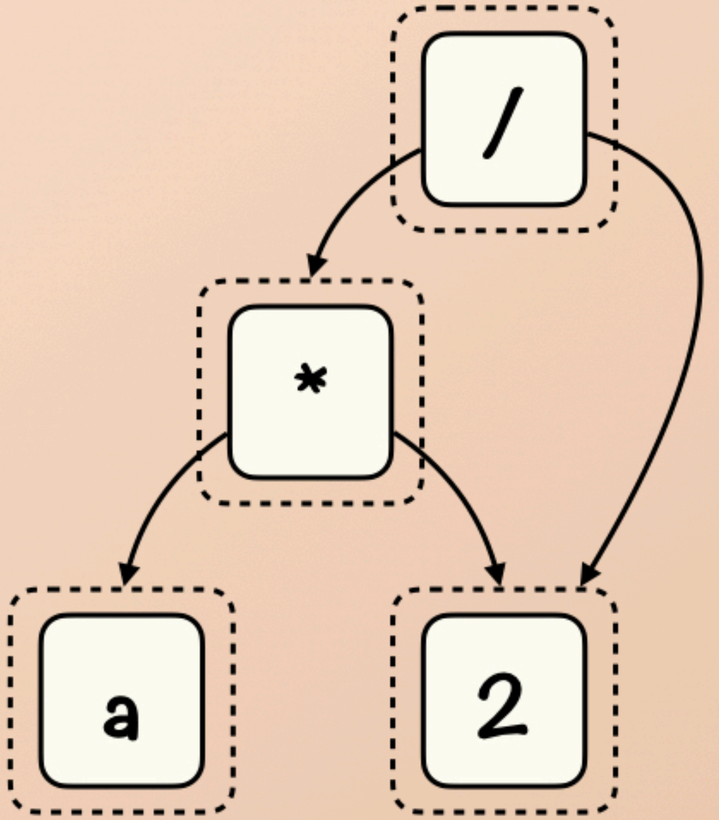


Sharing!

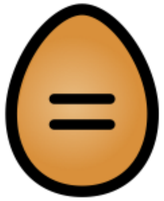


E-Graphs



eclass

enode



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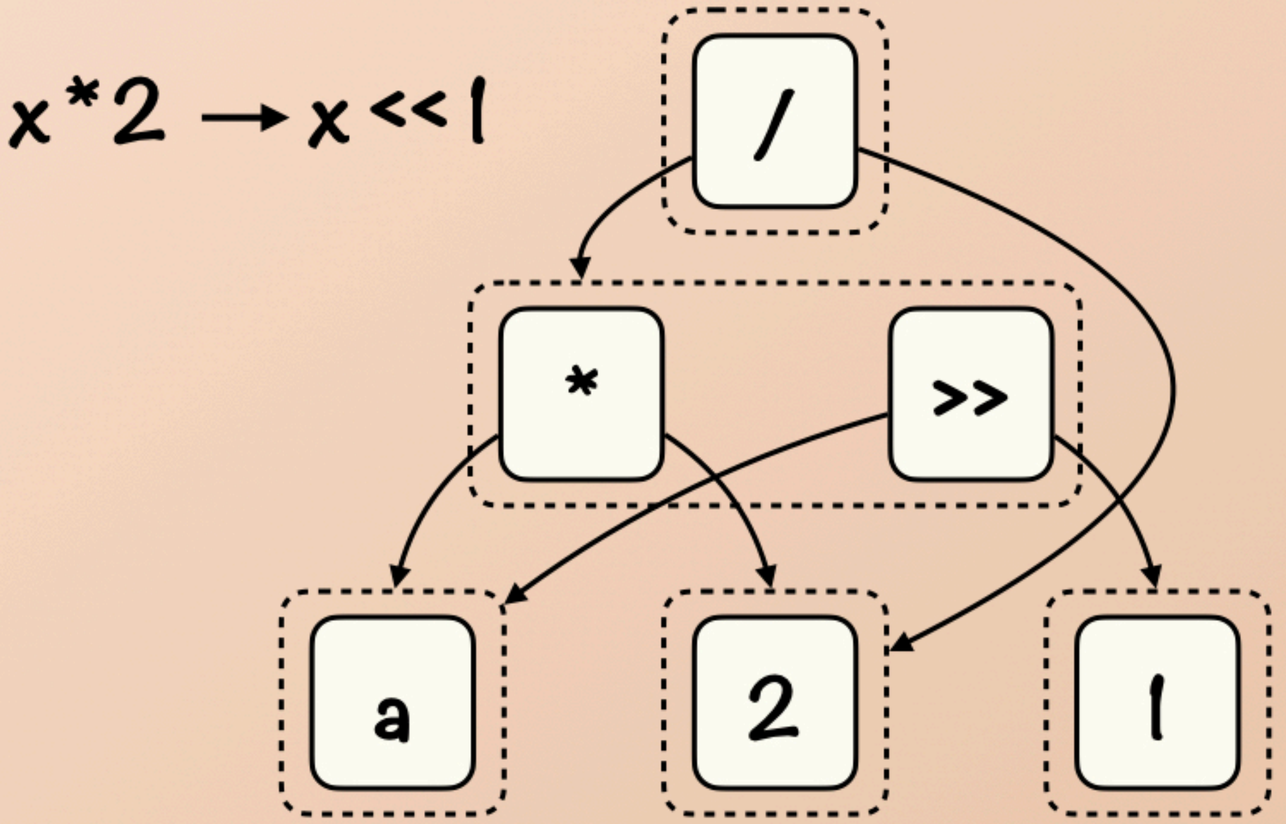
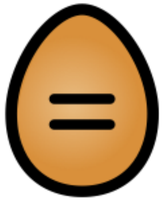




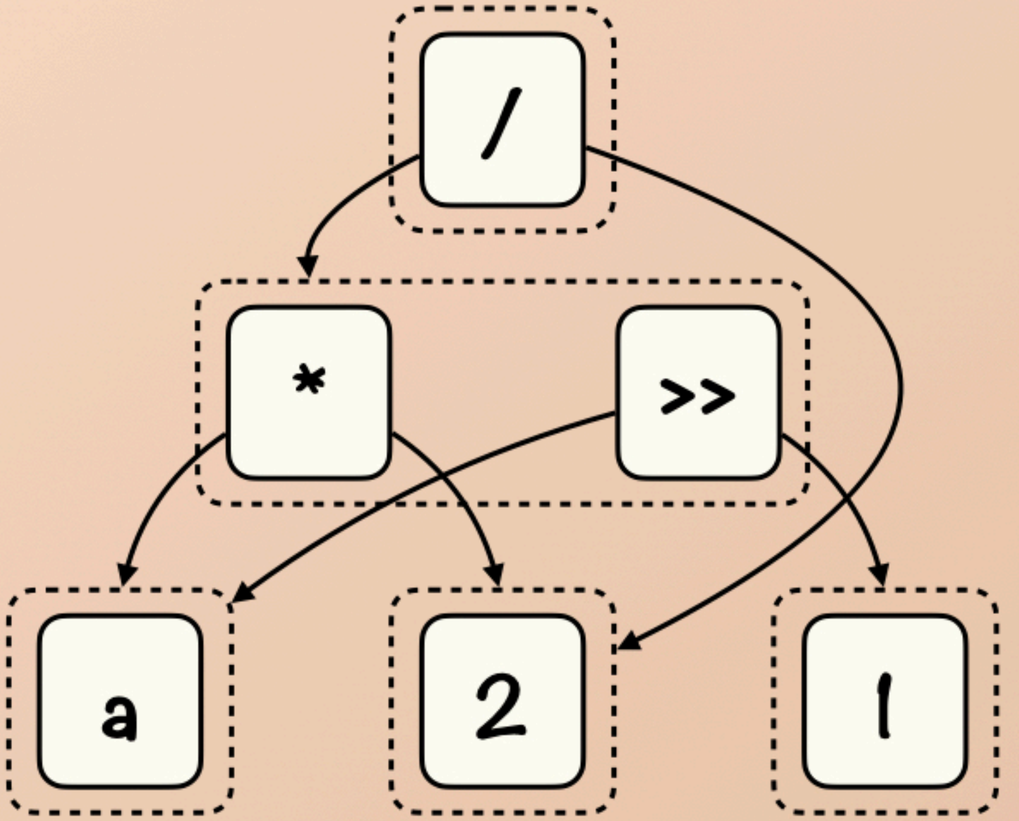
E-Graphs Never Forget

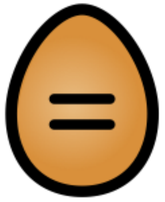
(a * 2) / 2

and

(a >> 1) / 2

are represented





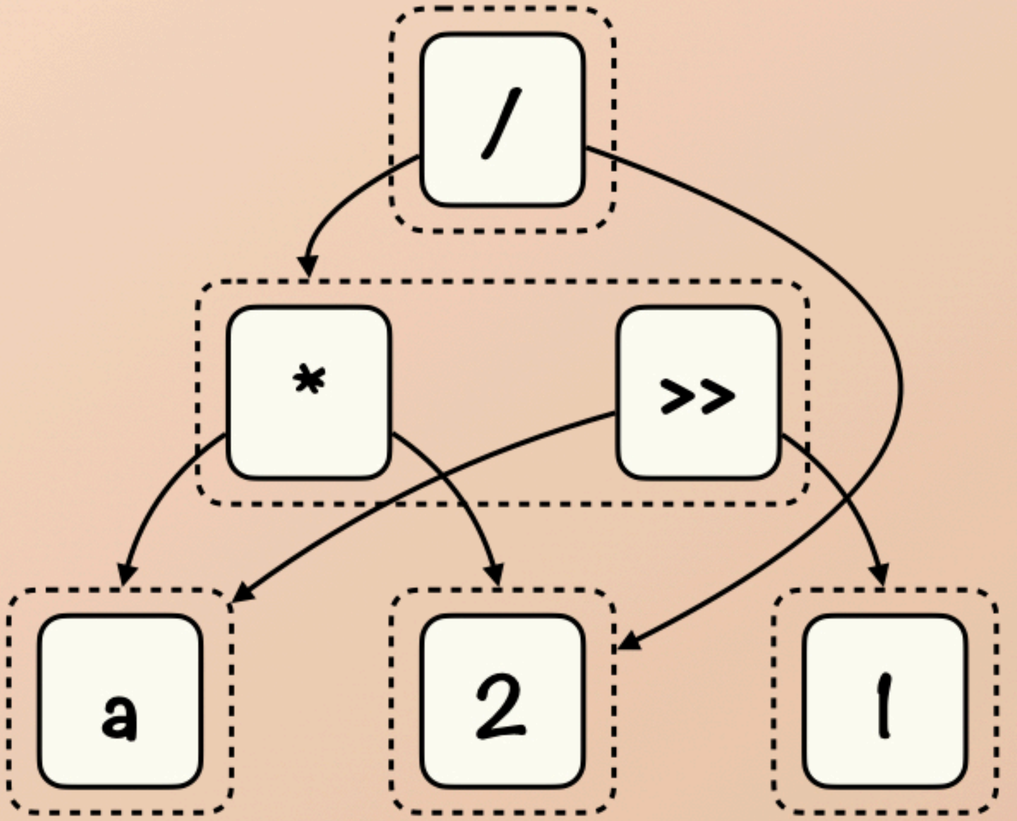
E-Graphs are Compact

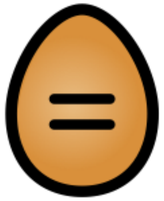
eclass sizes

$s_1, s_2, s_3 \ldots$

$\prod s_i$ terms

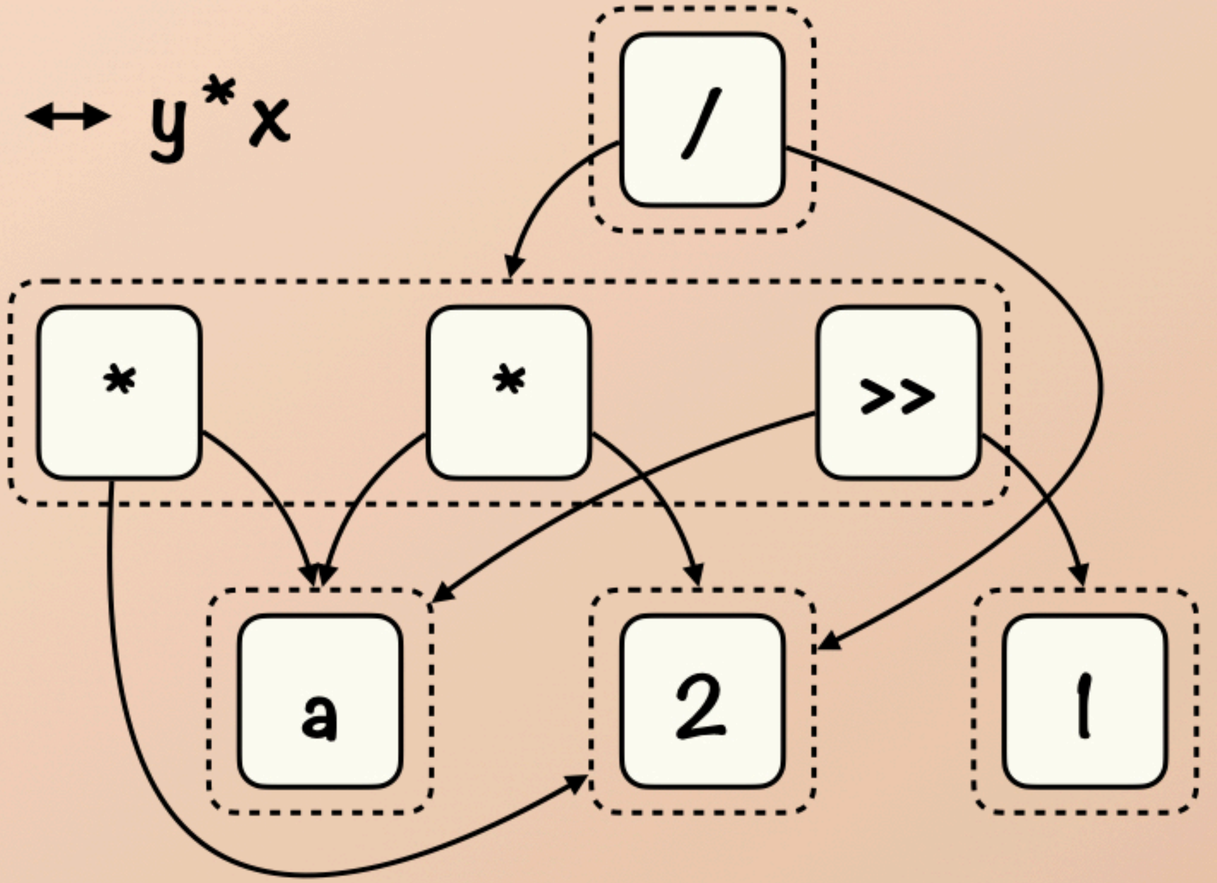
Σs_i space

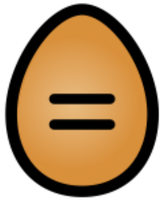




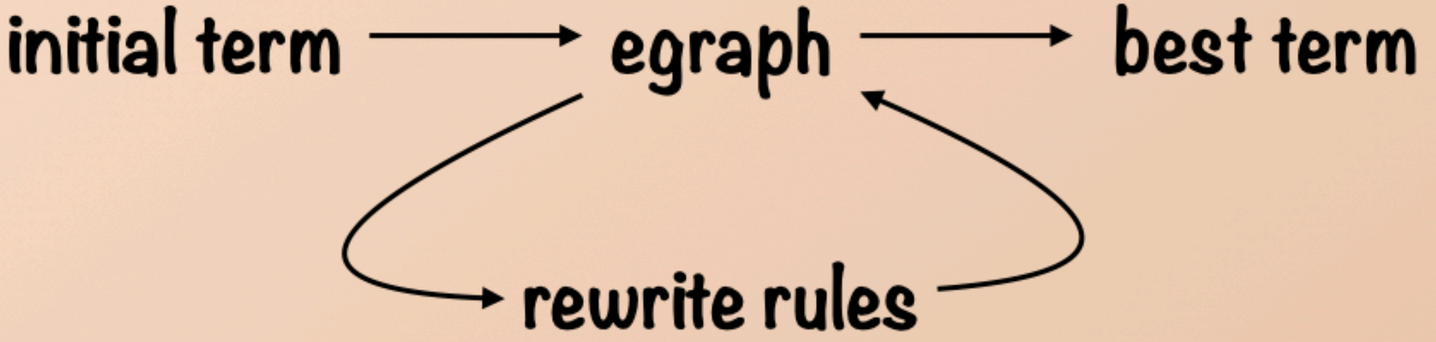
E-Graphs Can Saturate

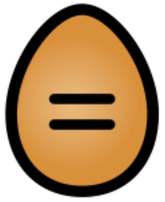
$x * y \leftrightarrow y * x$





Equality Saturation

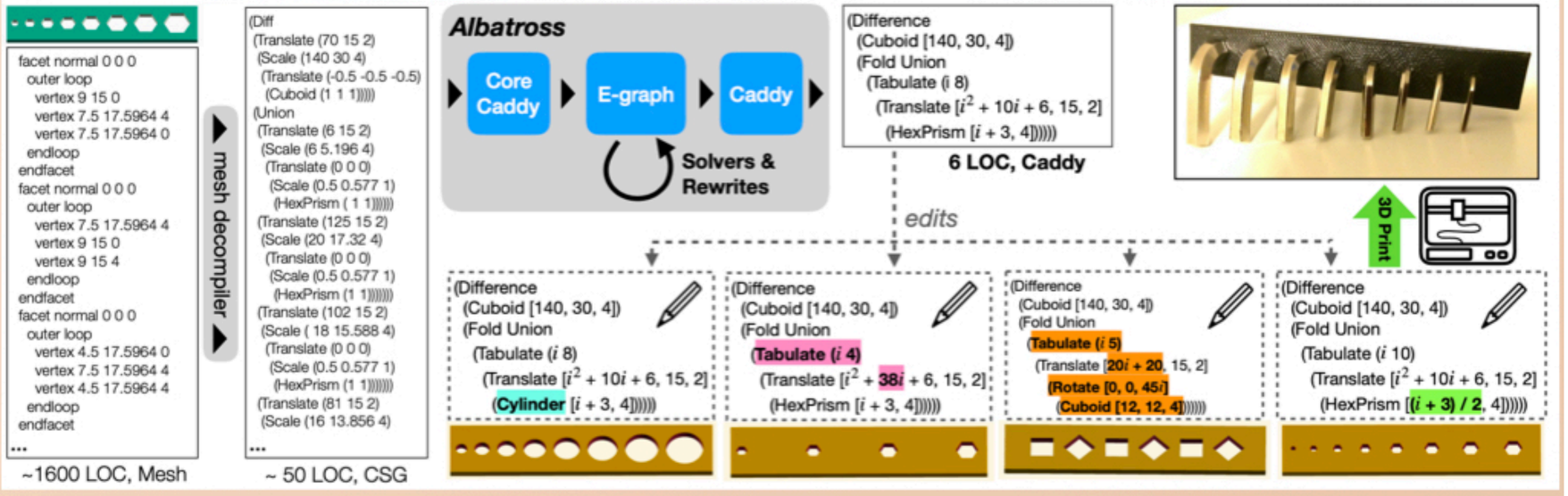




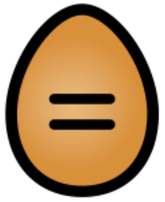
Herbie

- Uses E-Graphs to simplify expressions
- Total speed up: 2.77x
- Simplify speed up: 5-60x
- Better results!

CAD Simplification

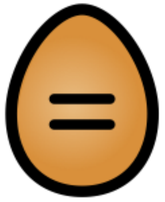


- Speed up >1000x
- Enabled a whole new set of techniques
- Discovered a new way on interacting with e-graphs



Linear Algebra Optimization

- Based on Apache SystemML
- Replace the optimization of LA expressions with E-Graph
- Extraction aware of density/memory-usage
- 1.2x - 5x better results



Using E-Graphs for Optimization with egg

Max Willsey

github.com/mwillsey/egg

Remy Wang Chandrakana Nandi Oliver Flatt

Pavel Panchekha Zach Tatlock

Why egraphs?

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Fundamentally, this is a problem of generating **many equivalent programs**—perfect for egraphs!

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However, in our case, “programs” will simultaneously represent both hardware *and* software!

Rewrites over our programs then become a natural way to represent changing the partition between hardware and software!

Glenside's goal:

For a given deep learning workload, efficiently explore the massive space of accelerator designs using egraphs.

Glenside Design

How Glenside Works

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Given: (1) A deep learning model in a high level deep learning DSL; (2) a library of *hardware atoms*

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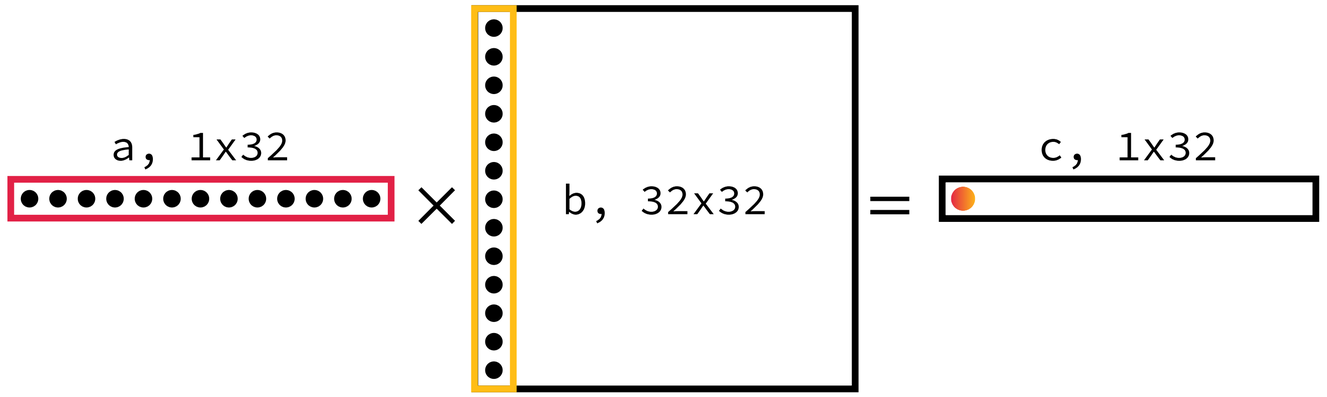
Our Workload: Vector–Matrix Multiply



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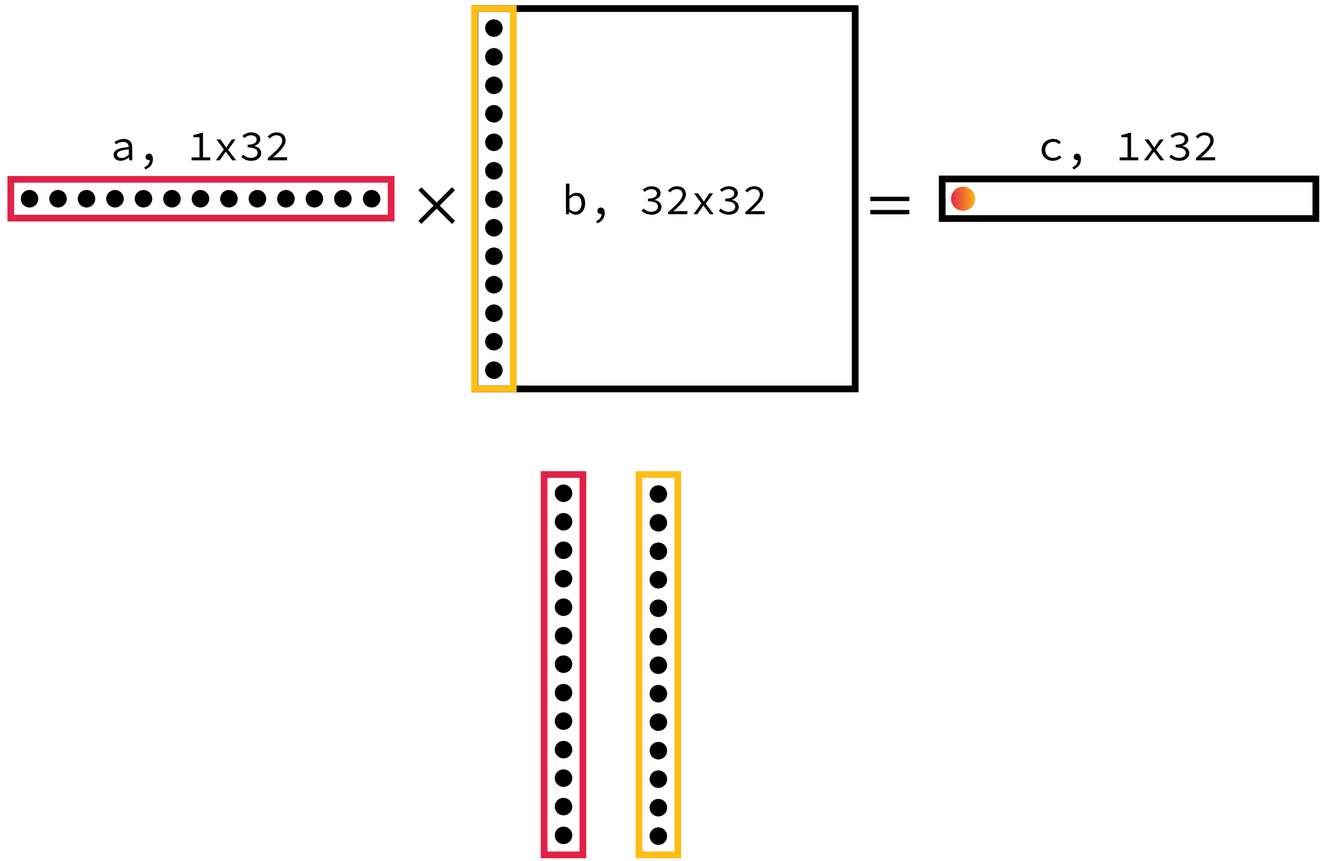

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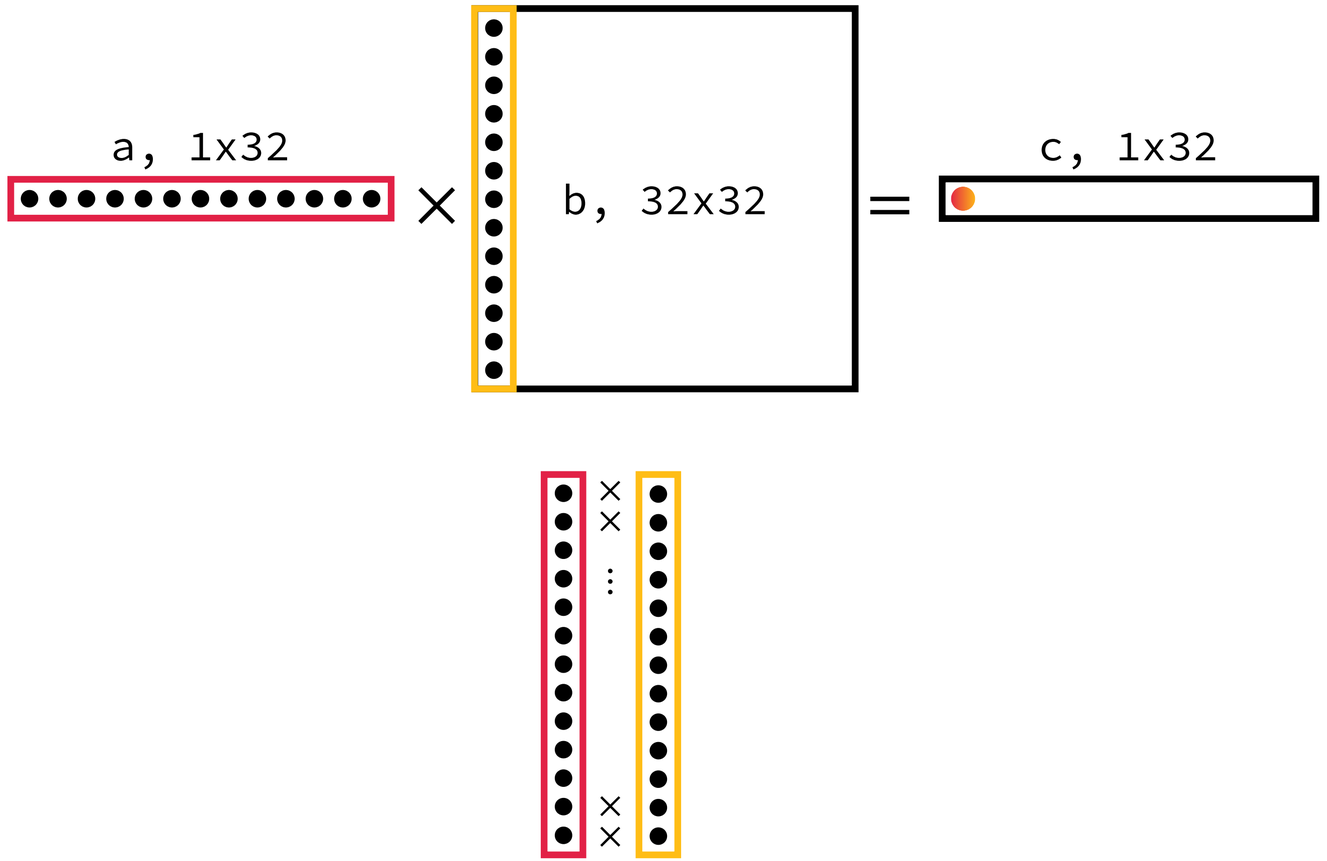

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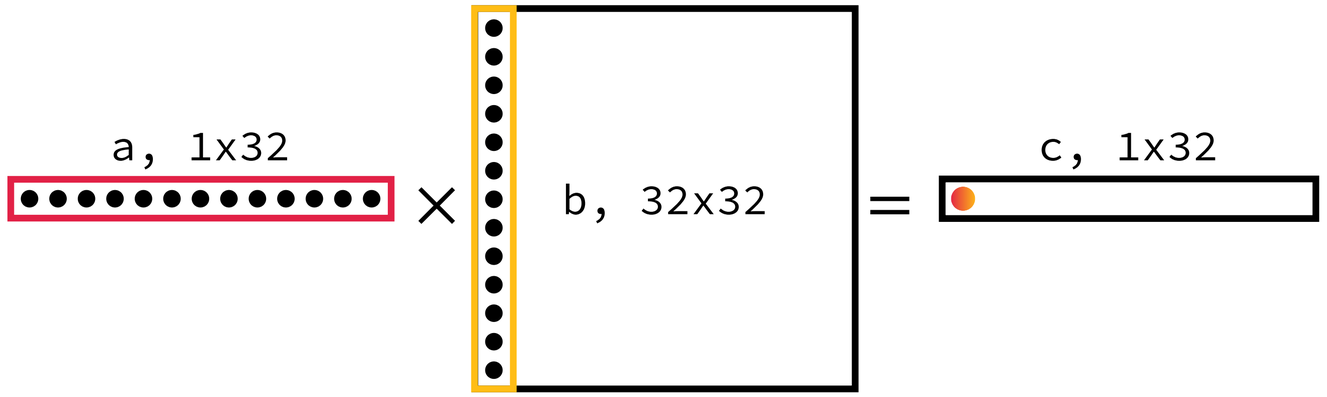

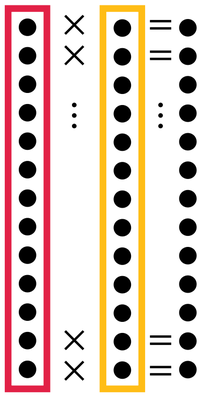

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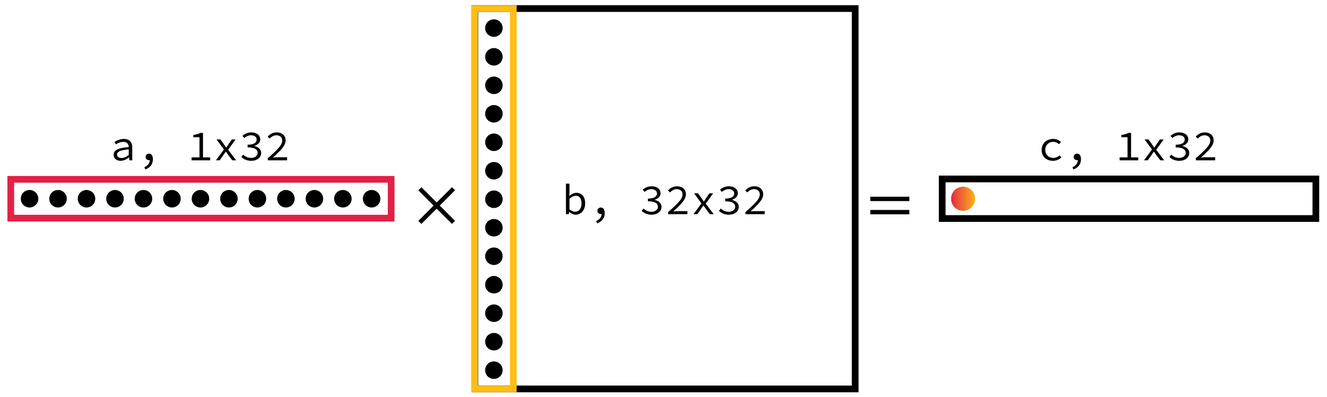

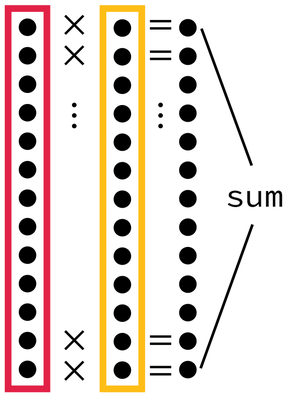

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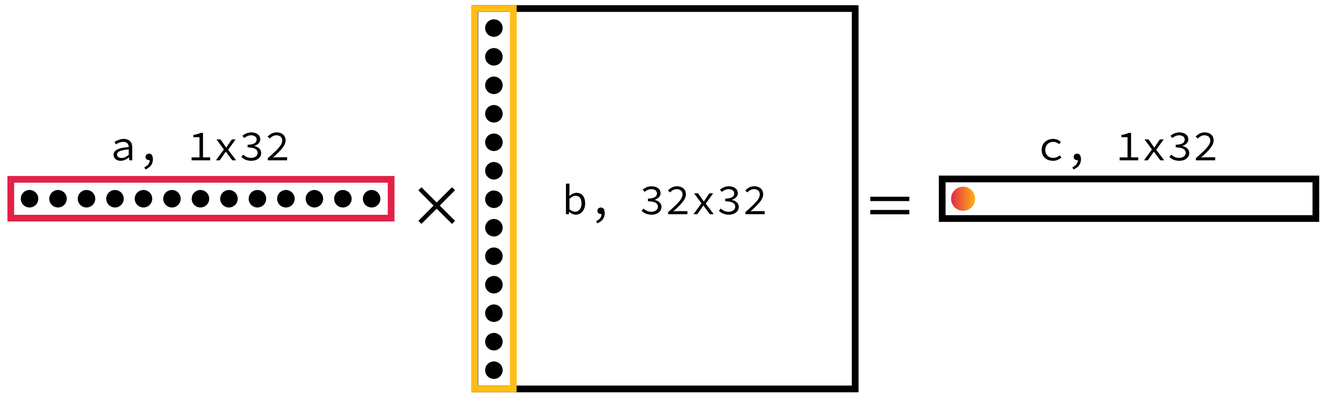

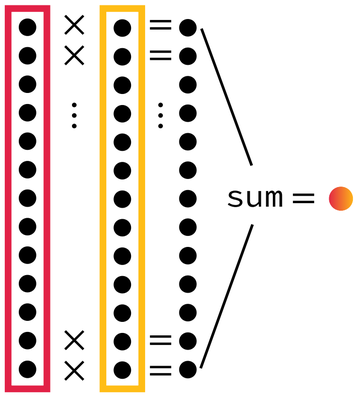

How do we represent vector–matrix multiplication in an egraph?

Egraph Representation

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For this to be possible, we need a representation where **every node has a value** and **there are no side-effects,** so that equivalent nodes can be swapped for one another (referential transparency).

```
(vec-mat-mult a b) :=
(map-dot-product
 (cartesian-product a (cols b))
)
```

Egraph Representation

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 (cartesian-product
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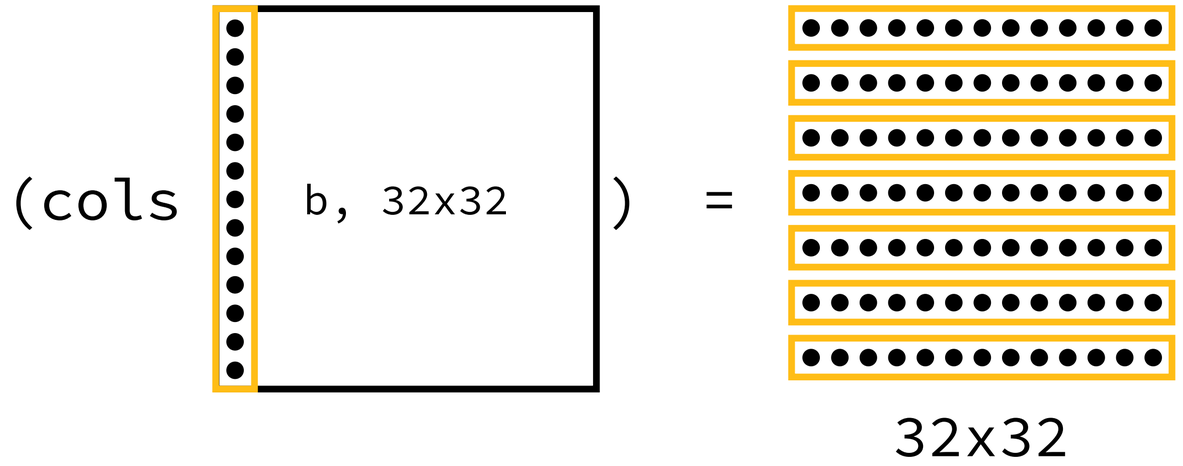

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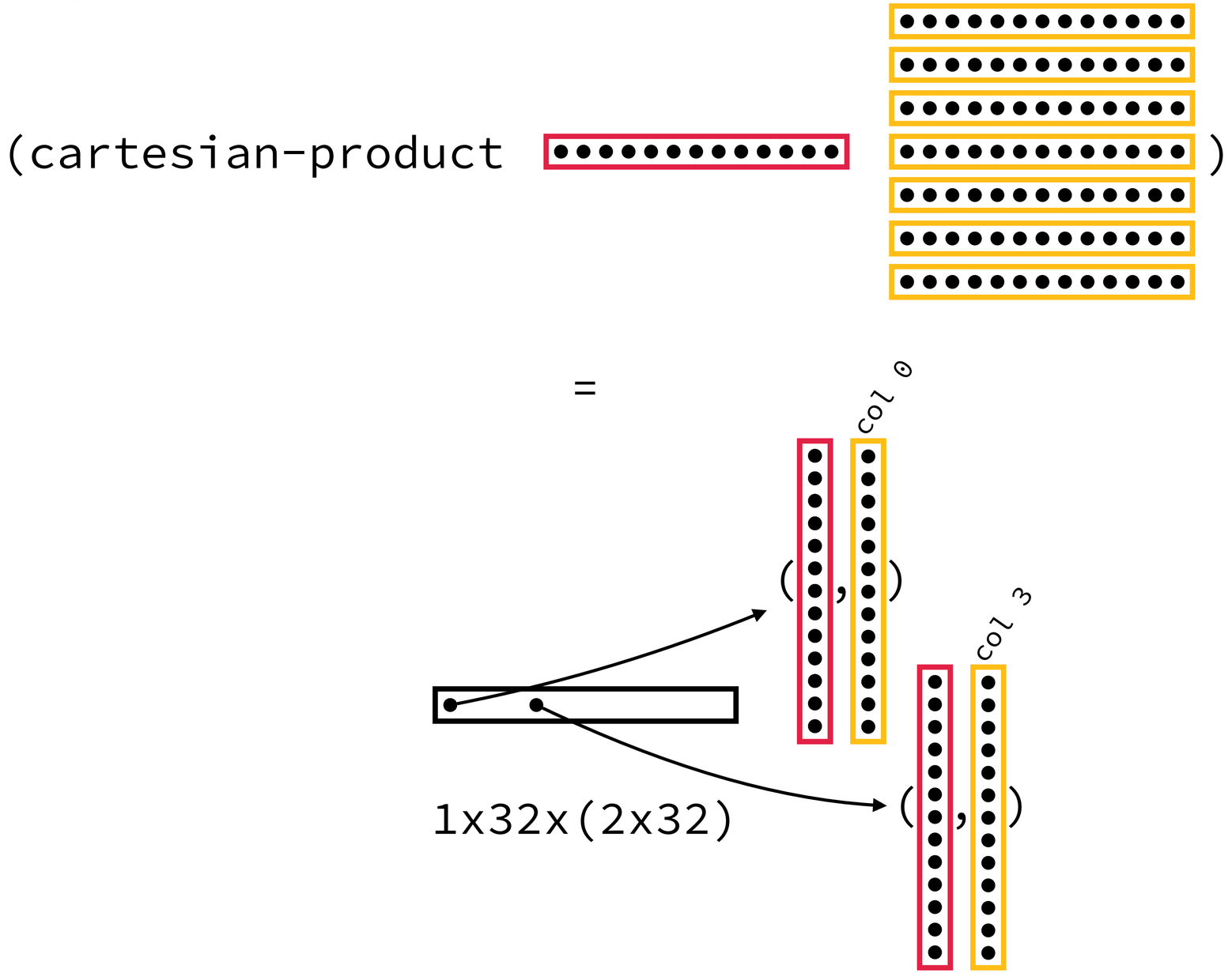

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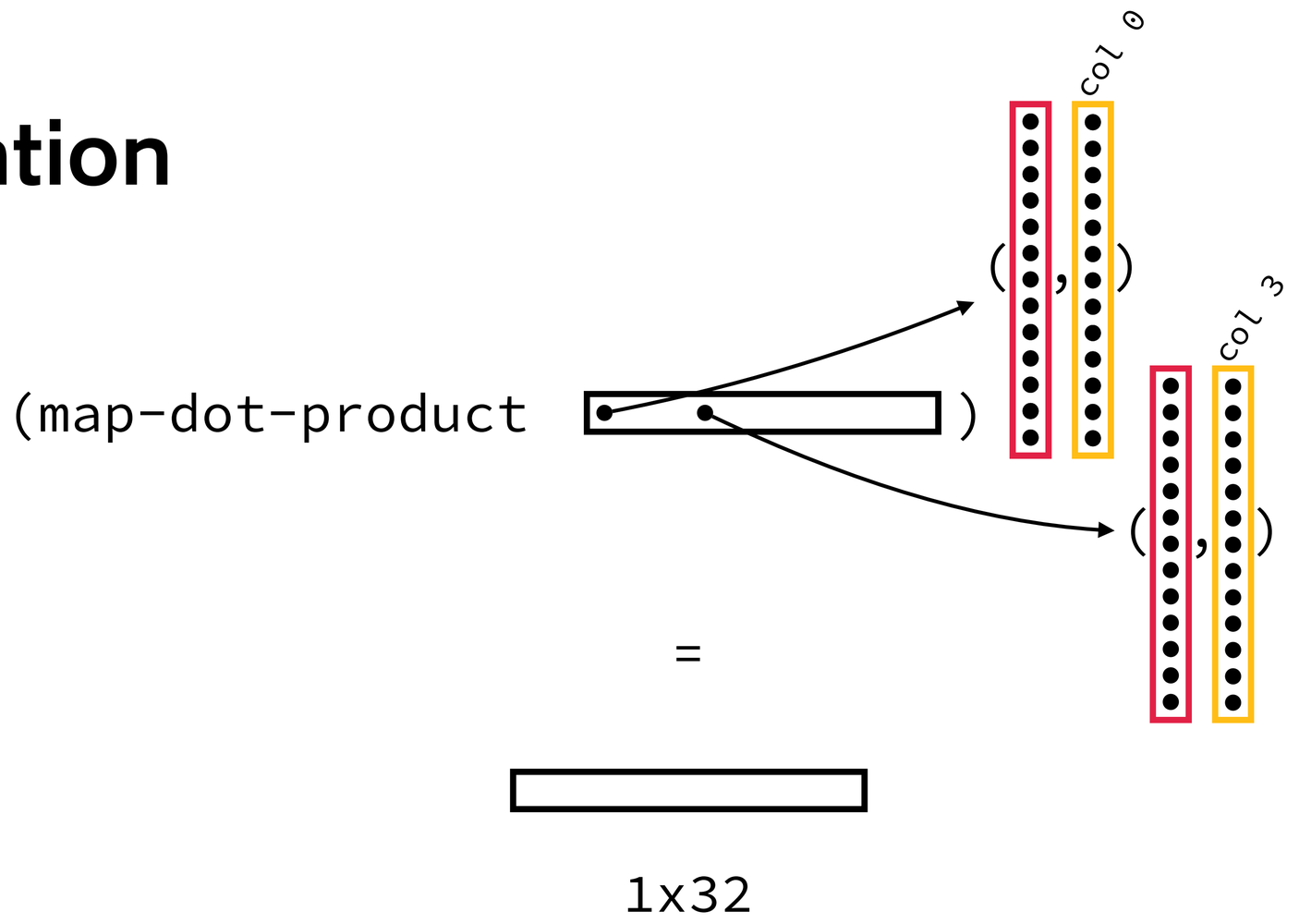

Hardware Atoms

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Hardware atoms are small hand-designed units which we compose to build a hardware design.

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Each hardware atom is paired with a functional description which we can use to map it in to the workload.

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Codesigning a Vector–Matrix Multiply

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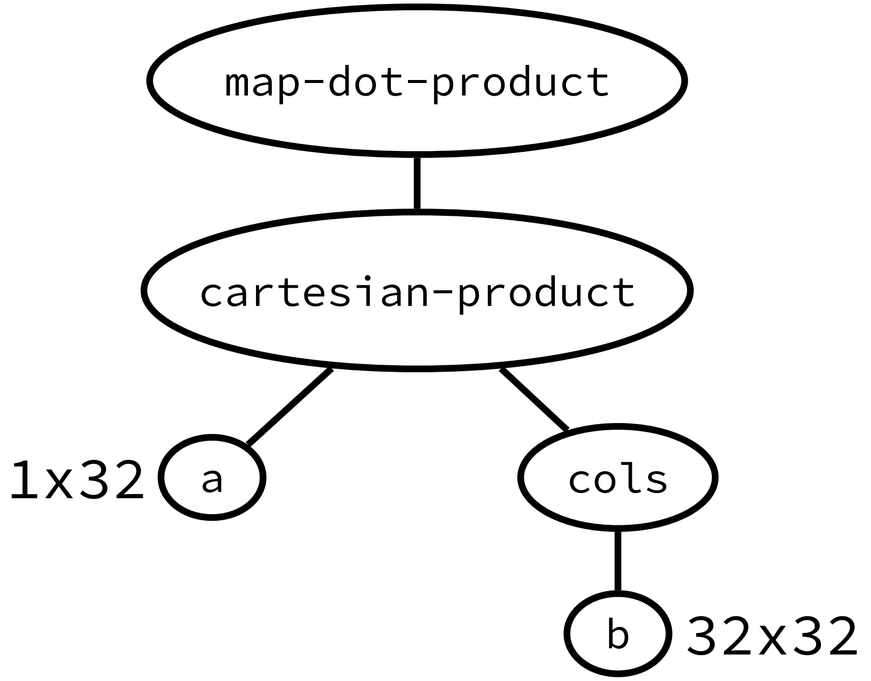
Where N,M = 16 or 32.



We have:

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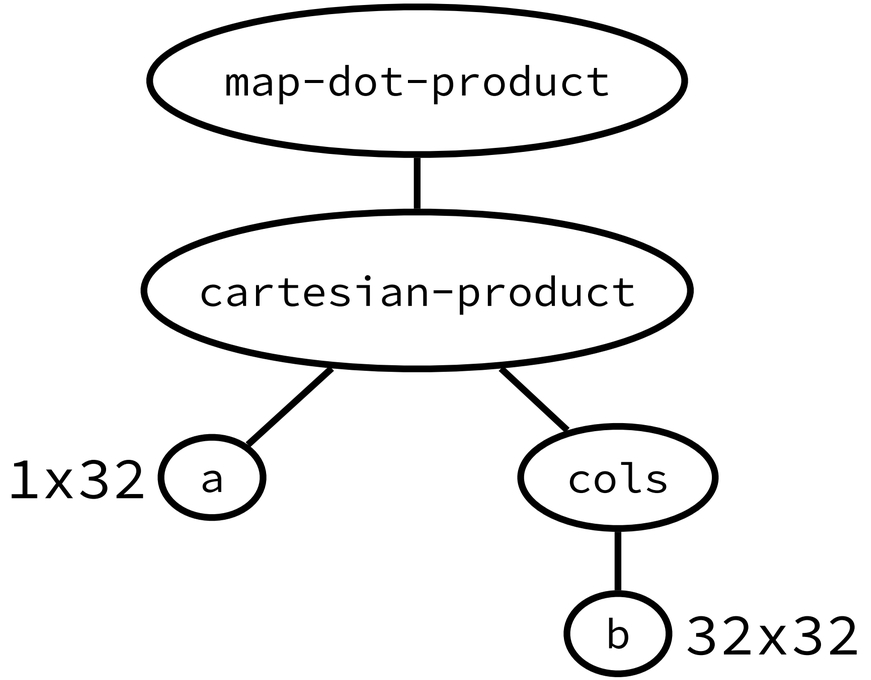
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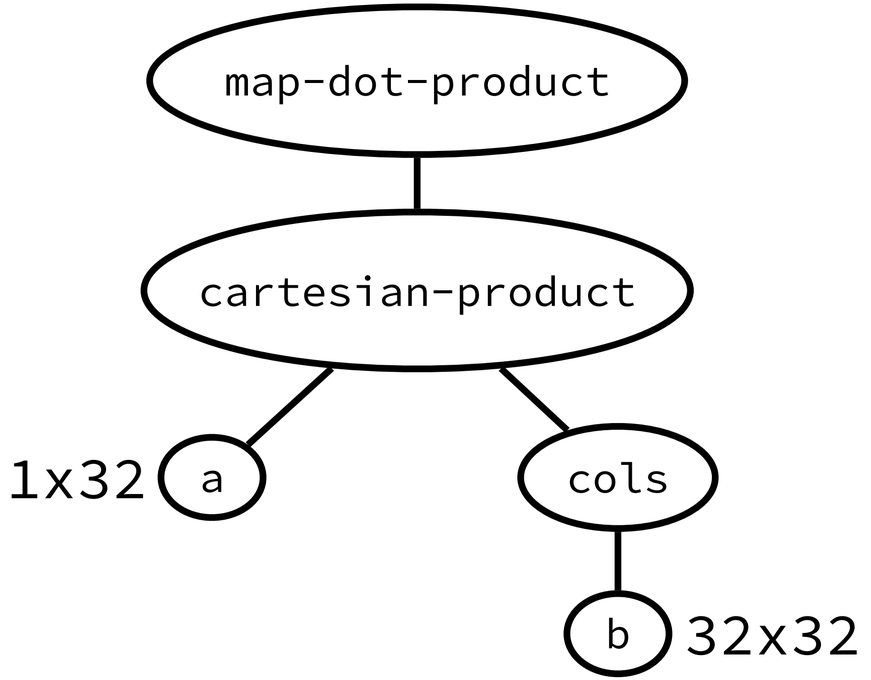
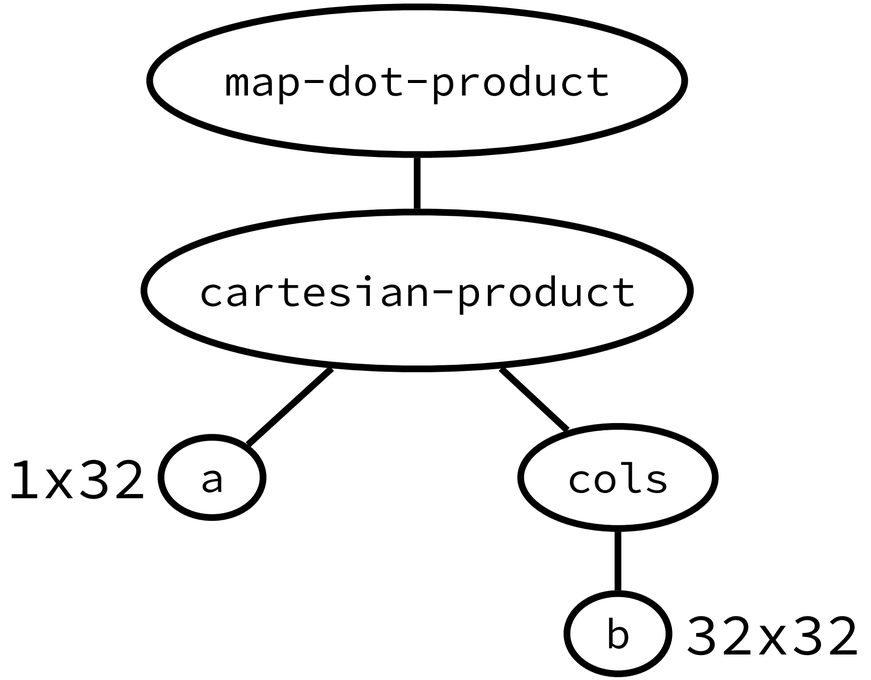
cartesian-product
1x32
a
cols
b
32x32



To explore hardware–software splits, we want to find places where we can introduce our hardware atom:



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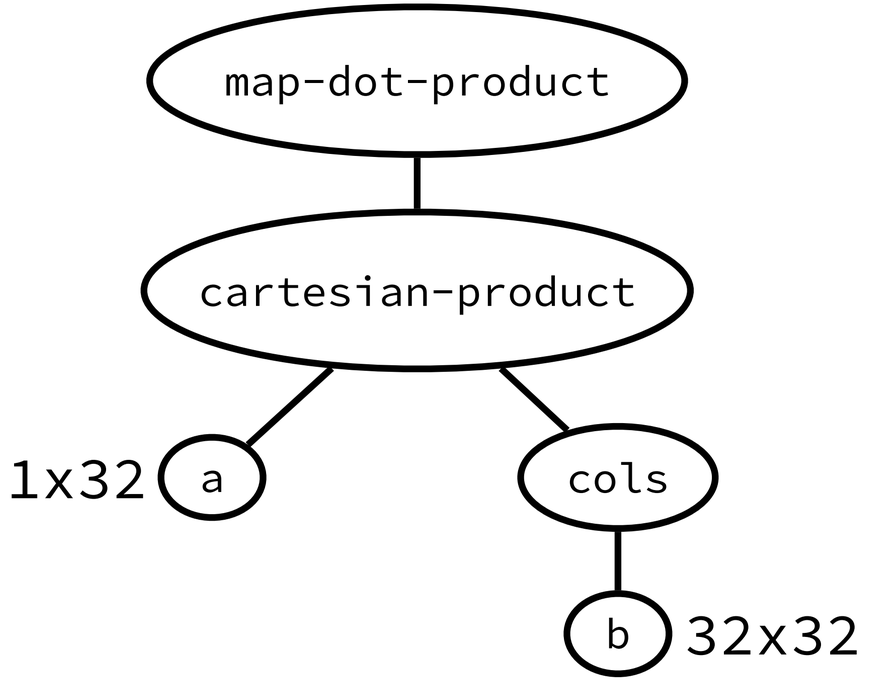

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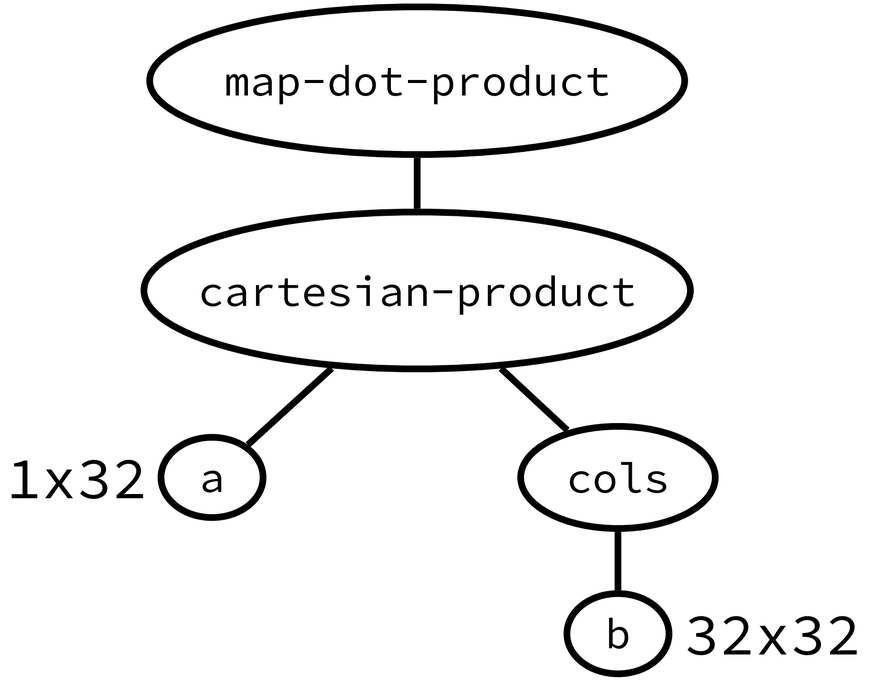

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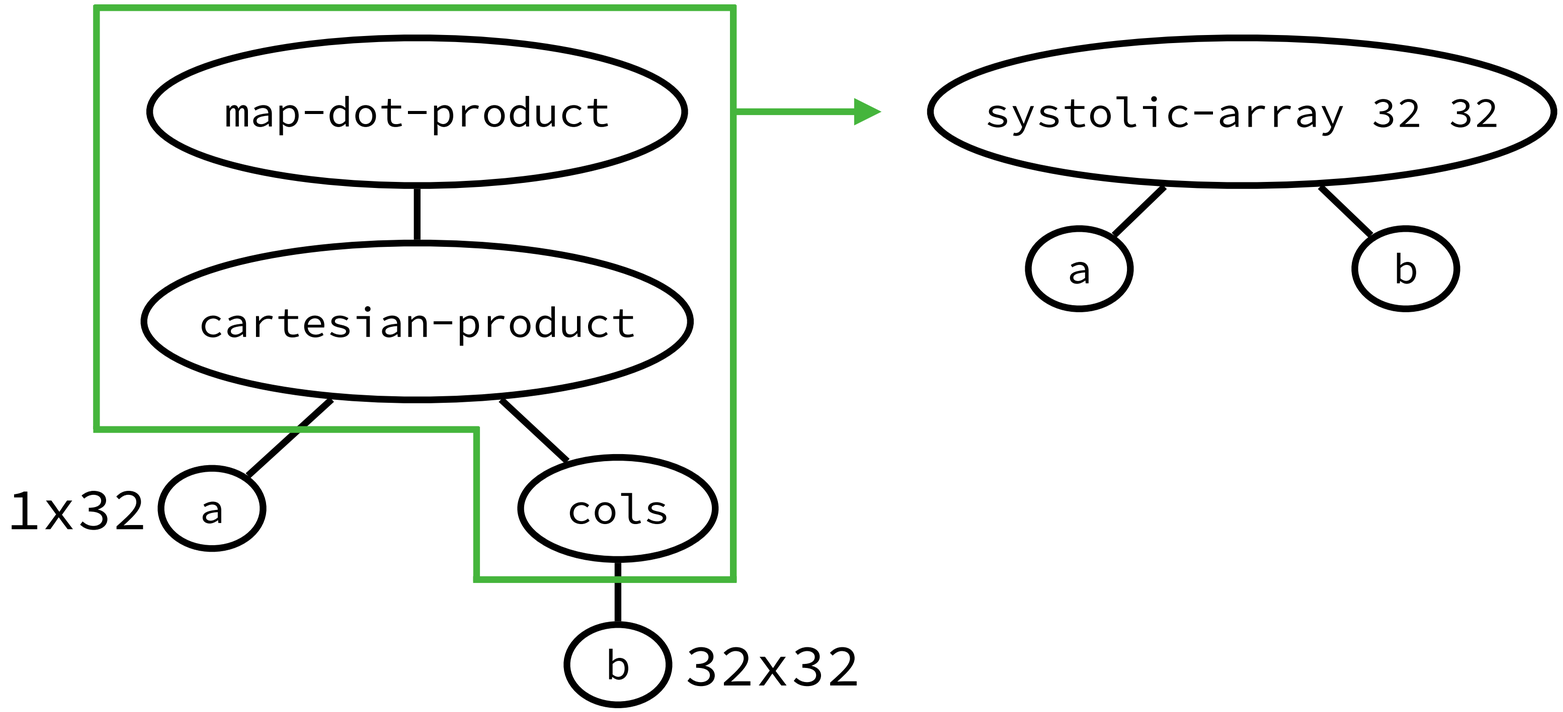

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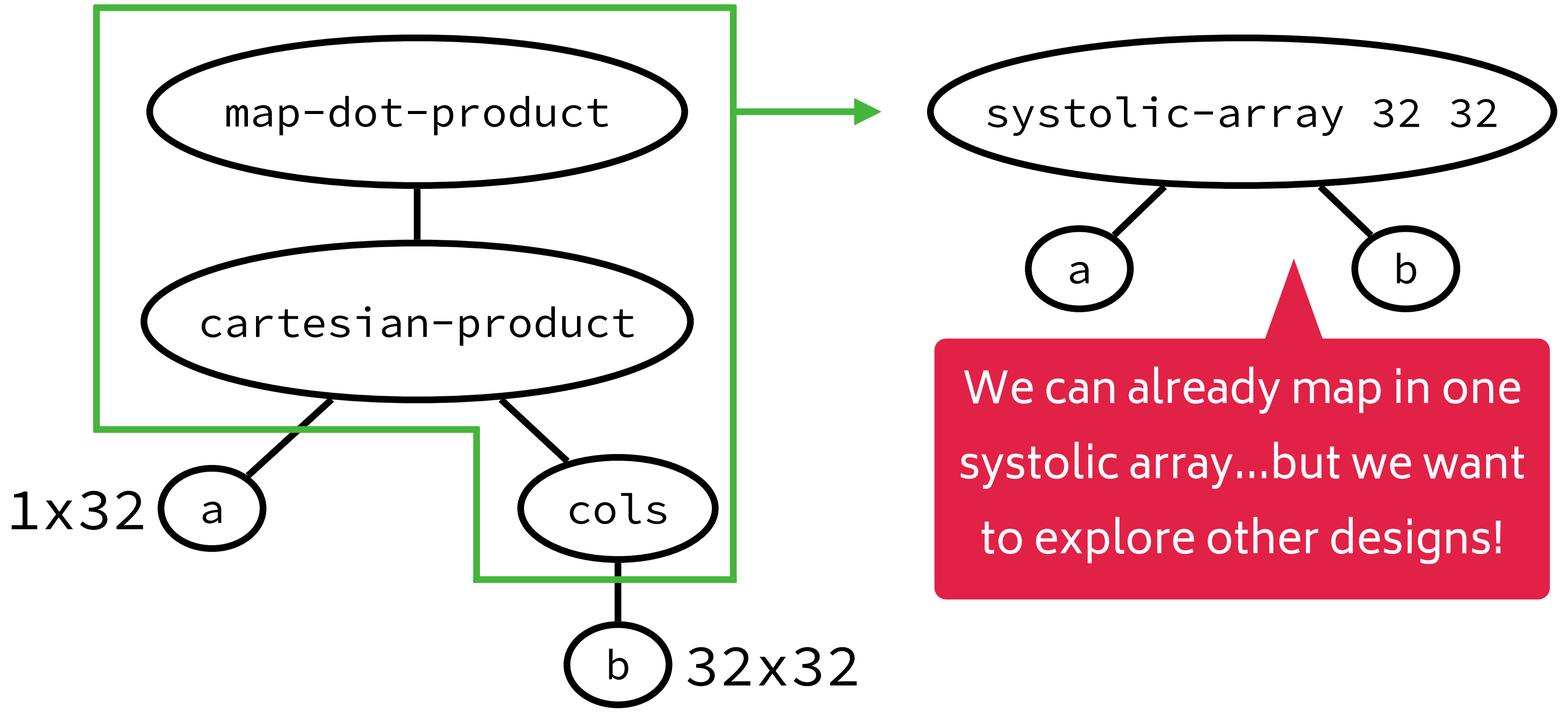

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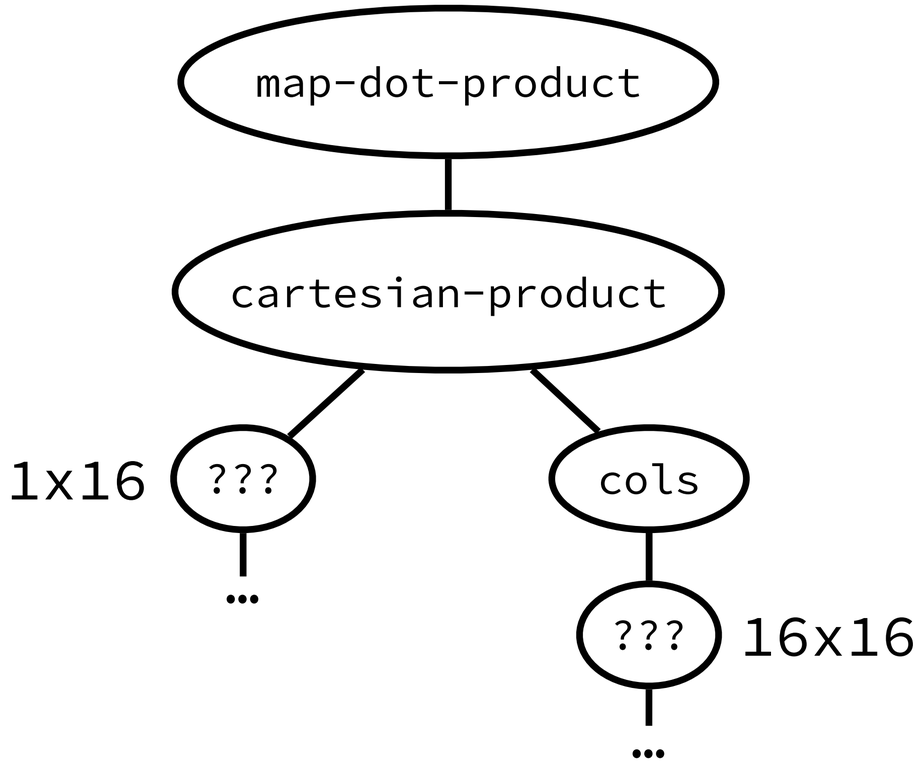
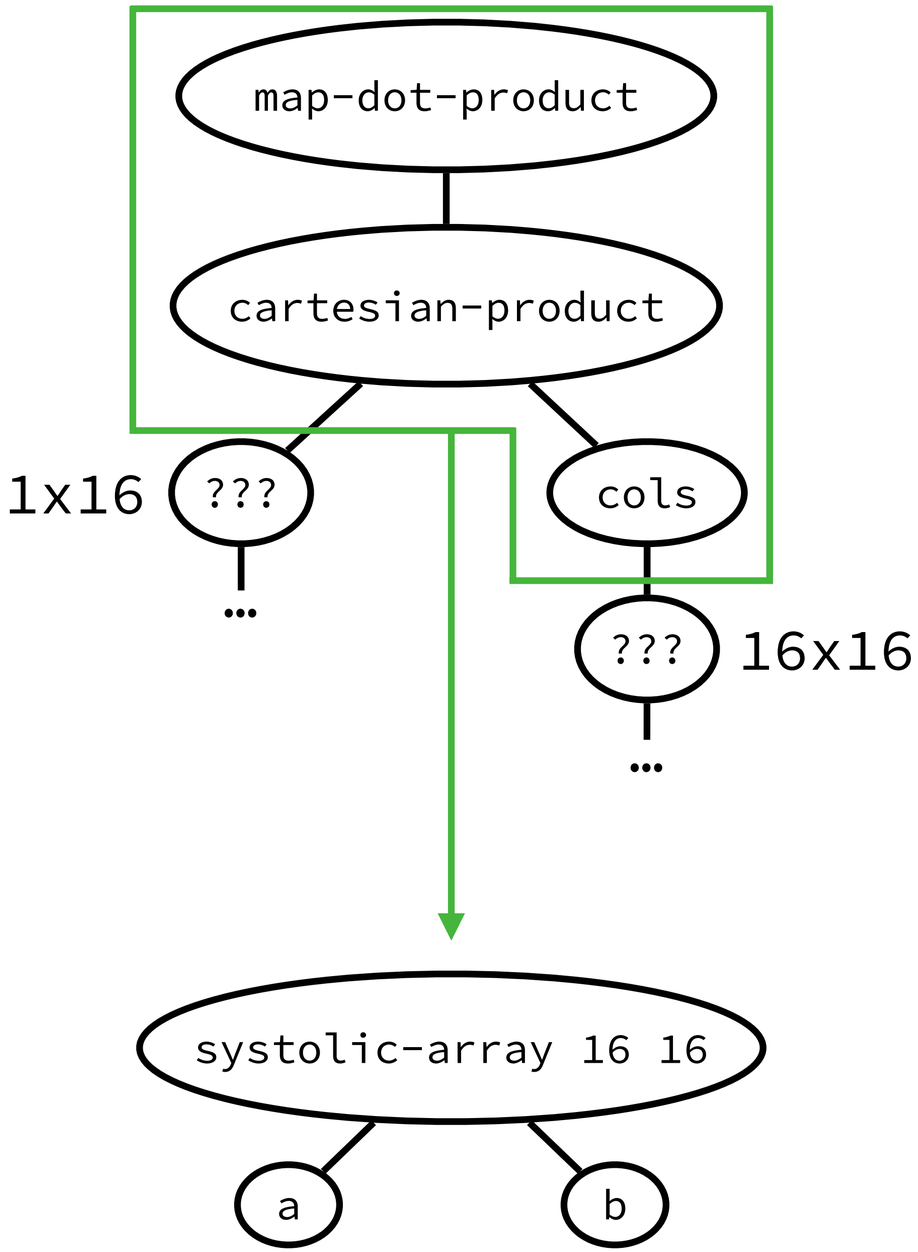
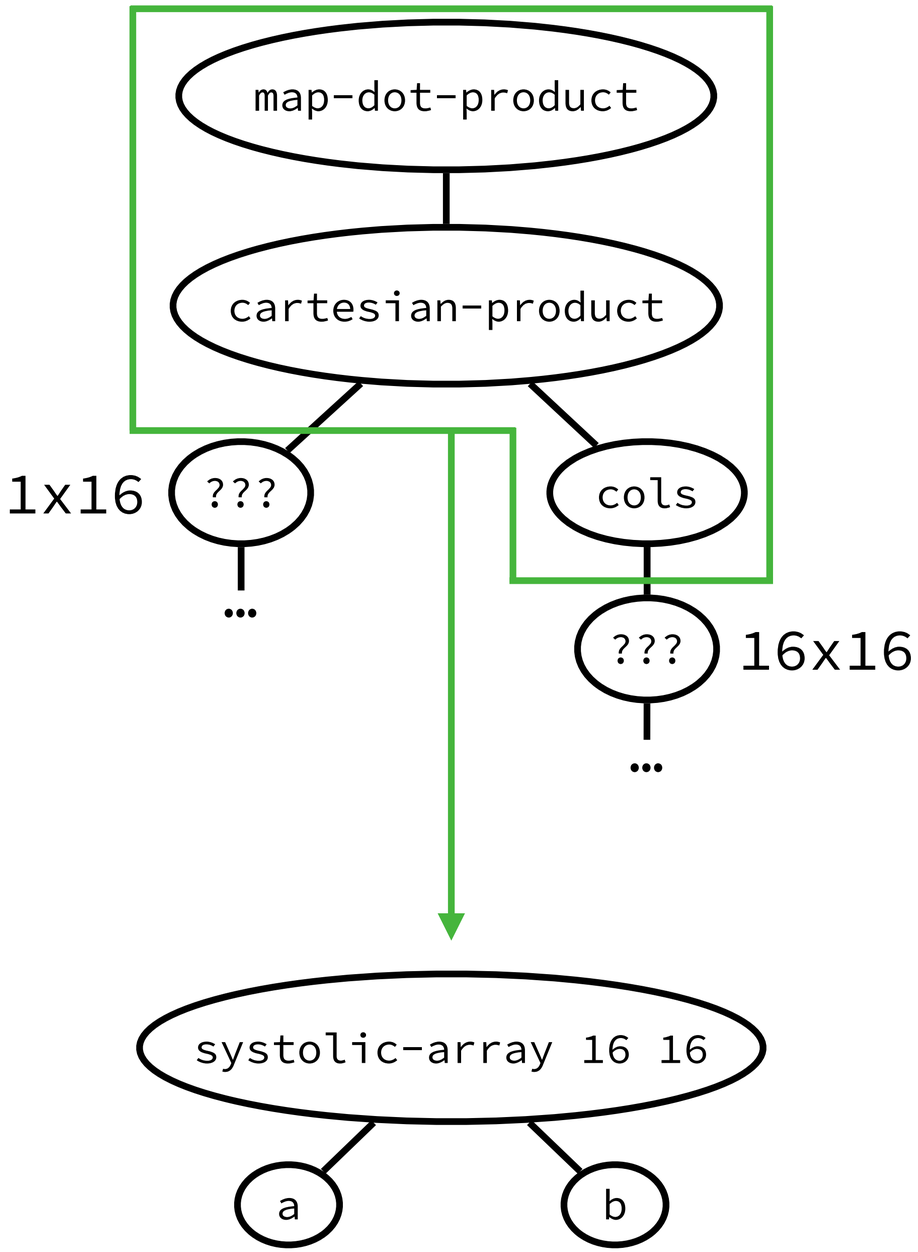

map-dot-product
cartesian-product
1x16
???
cols
???
16x16


map-dot-product
cartesian-product
1x16
???
...
cols
???
16x16
...
systolic-array 16 16
a
b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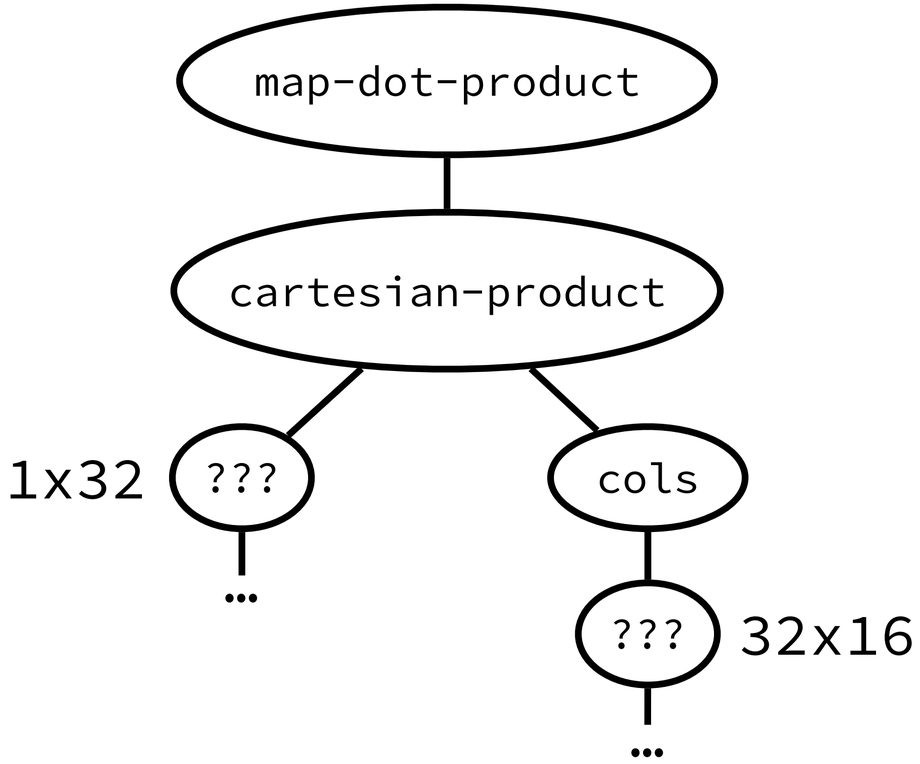
map-dot-product
cartesian-product
1x32
???
cols
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32x16
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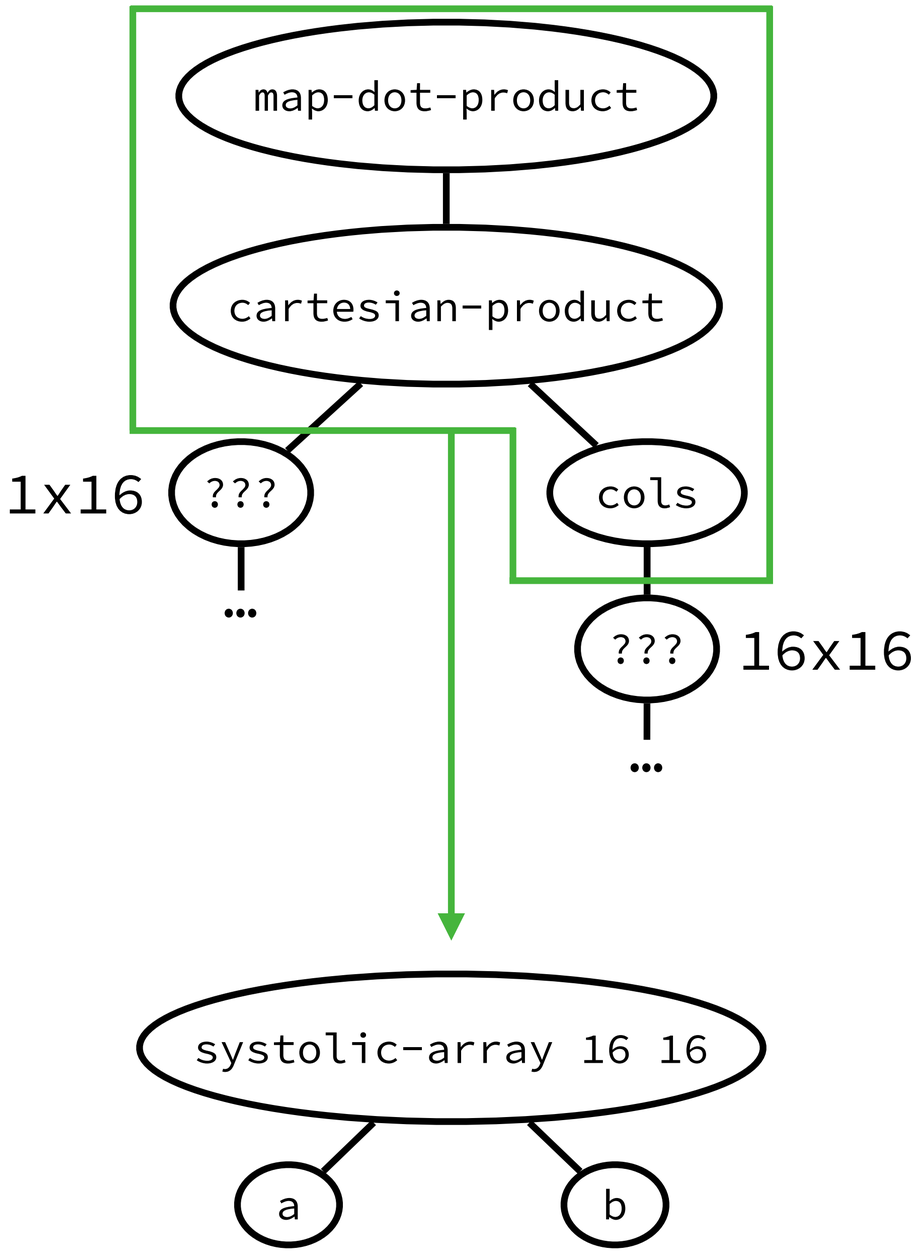
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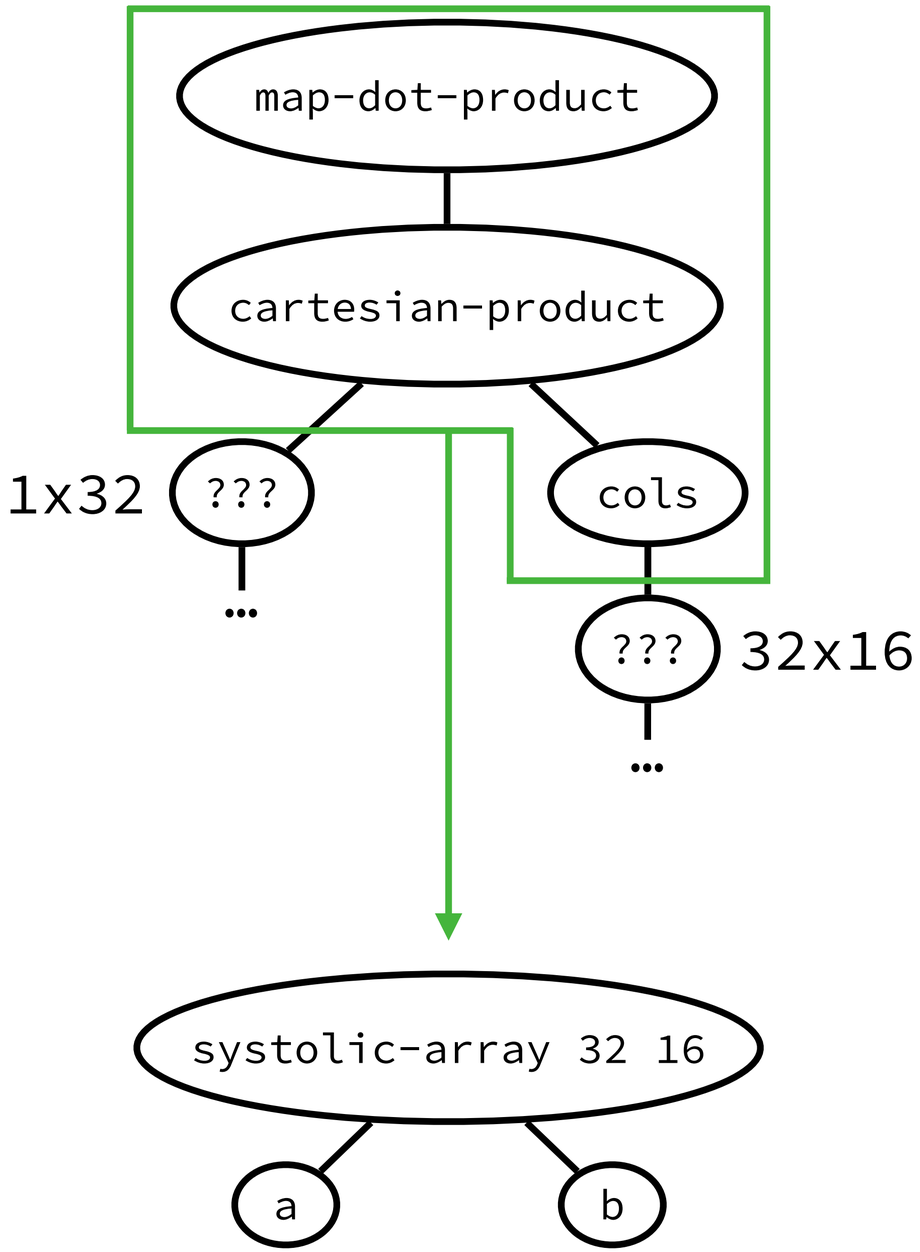
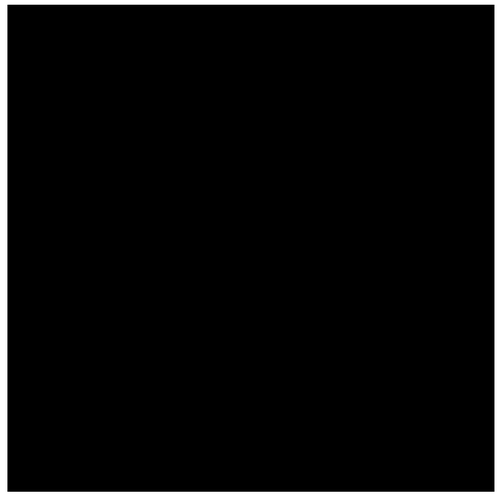

map-dot-product
cartesian-product
1x32
???
cols
???
32x16
systolic-array 32 16
a
b

We use rewrites to expose places where hardware can be mapped in!

First Rewrite: Splitting



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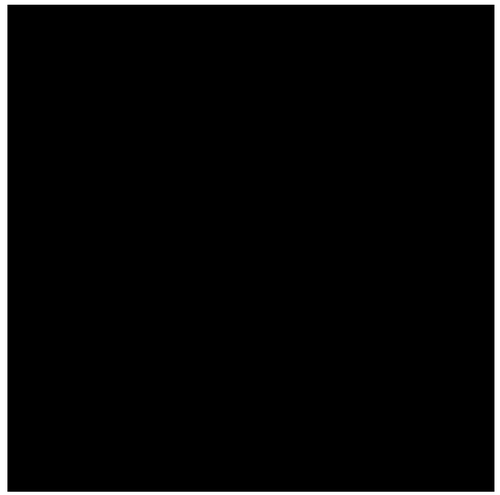

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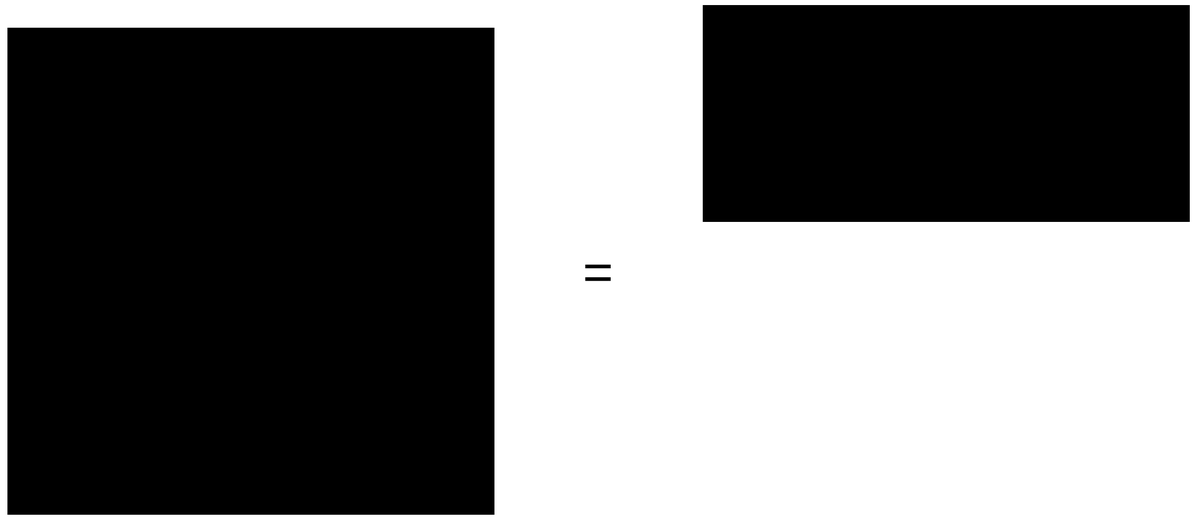

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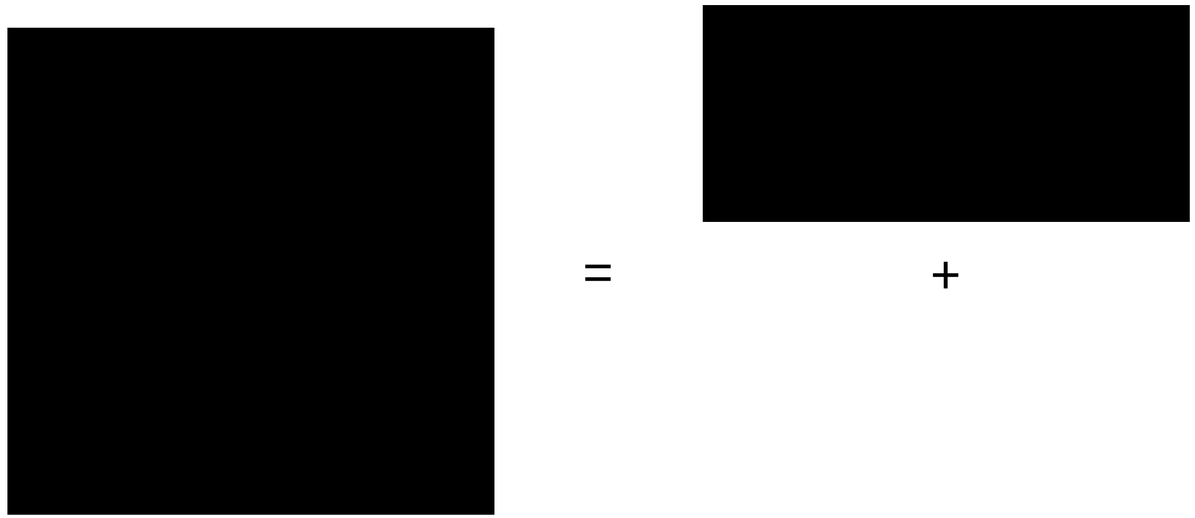
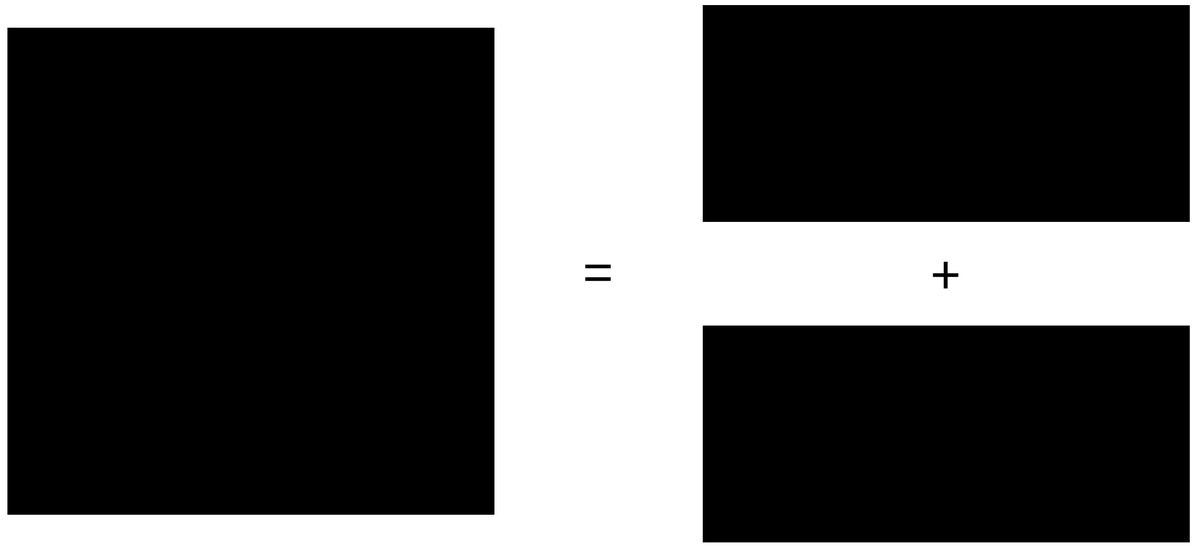
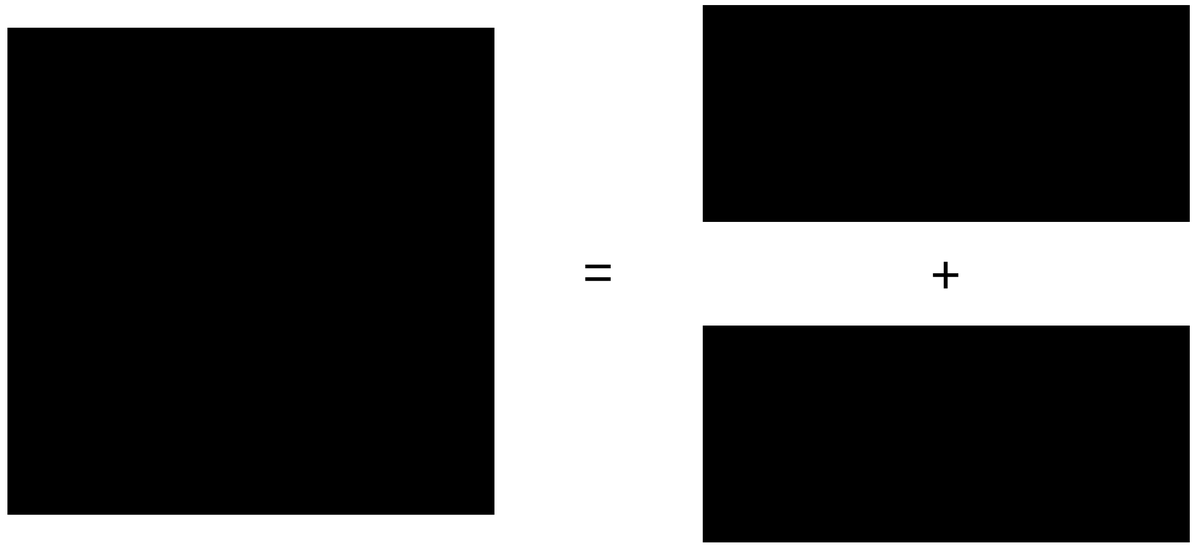


First Rewrite: Splitting

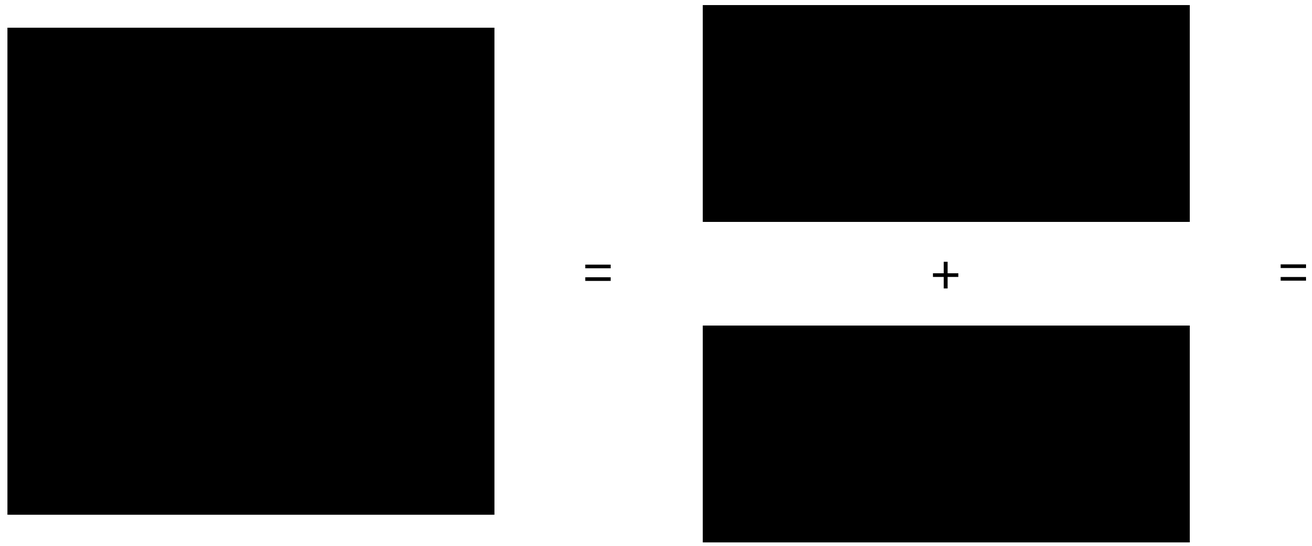


First Rewrite: Splitting




```
a => (concat (slice a ...) (slice a ...))
```

First Rewrite: Splitting




```
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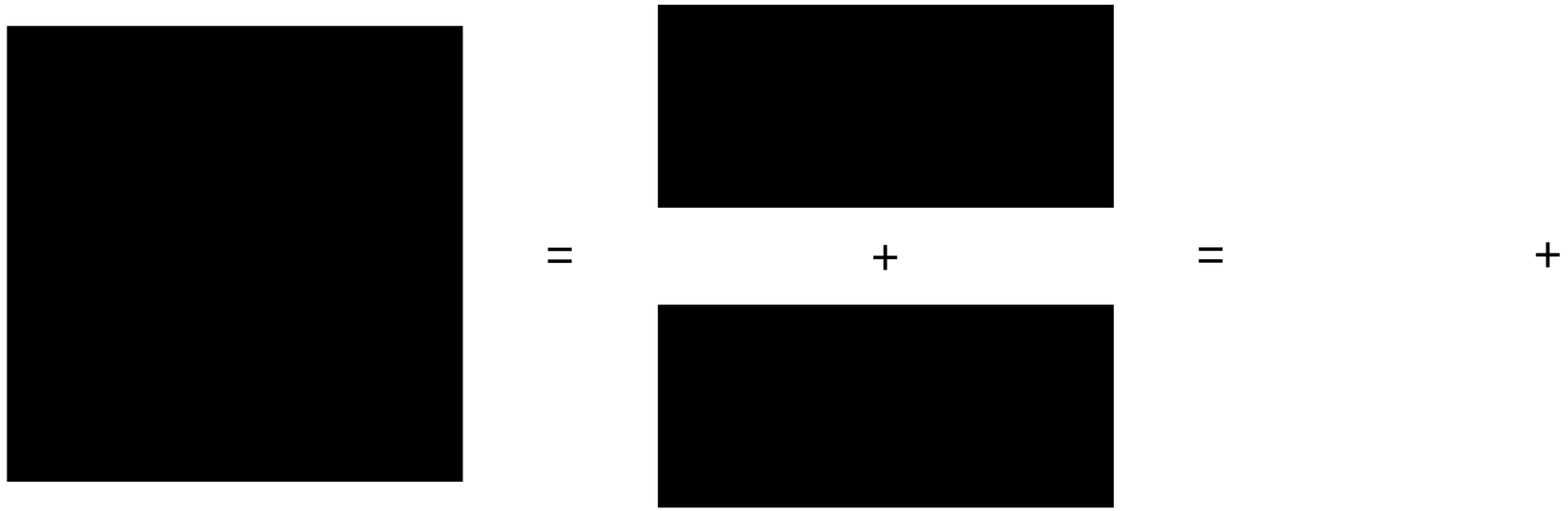


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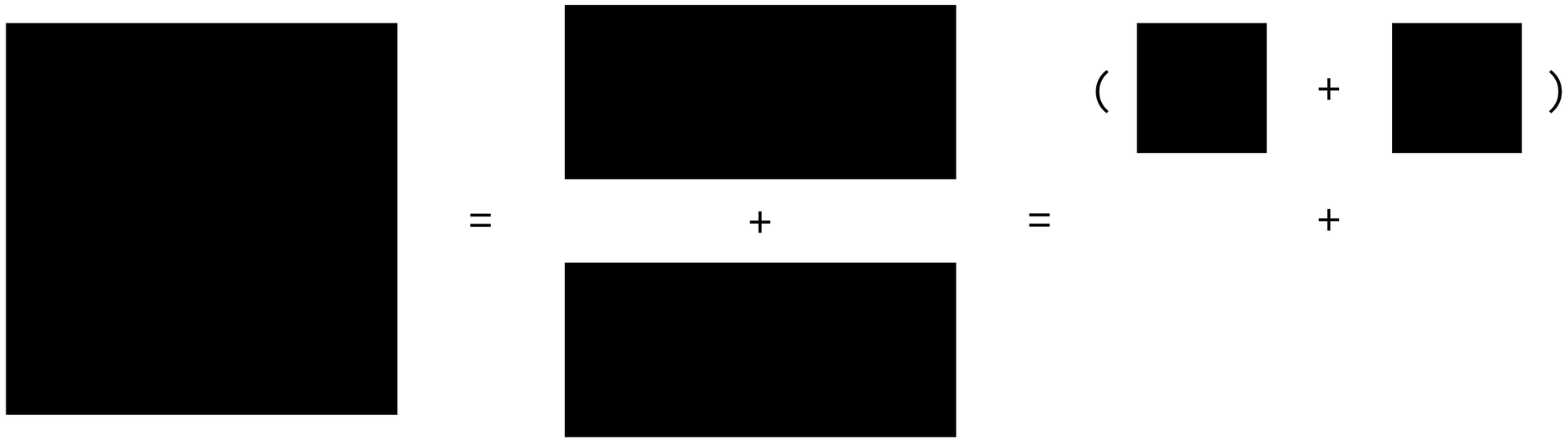


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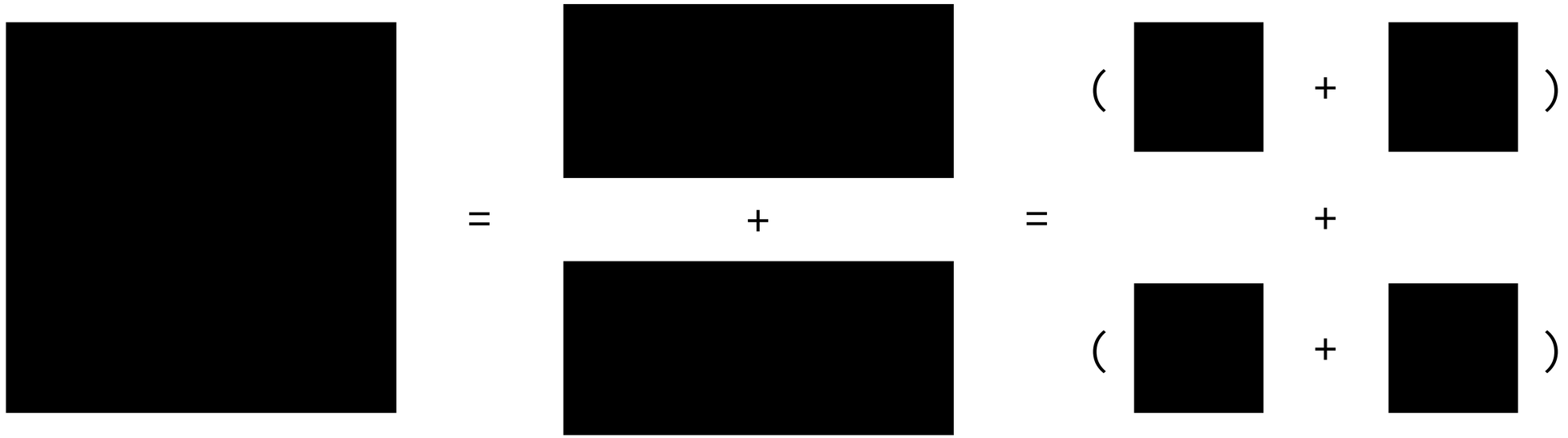


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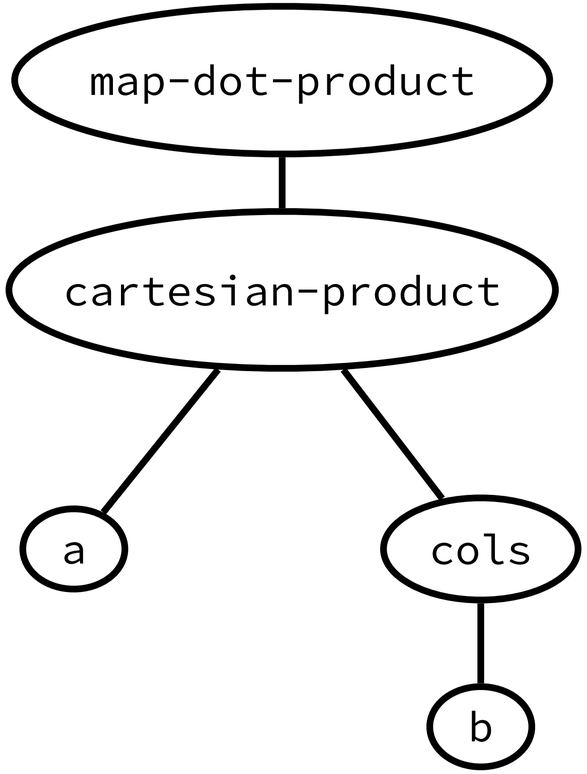
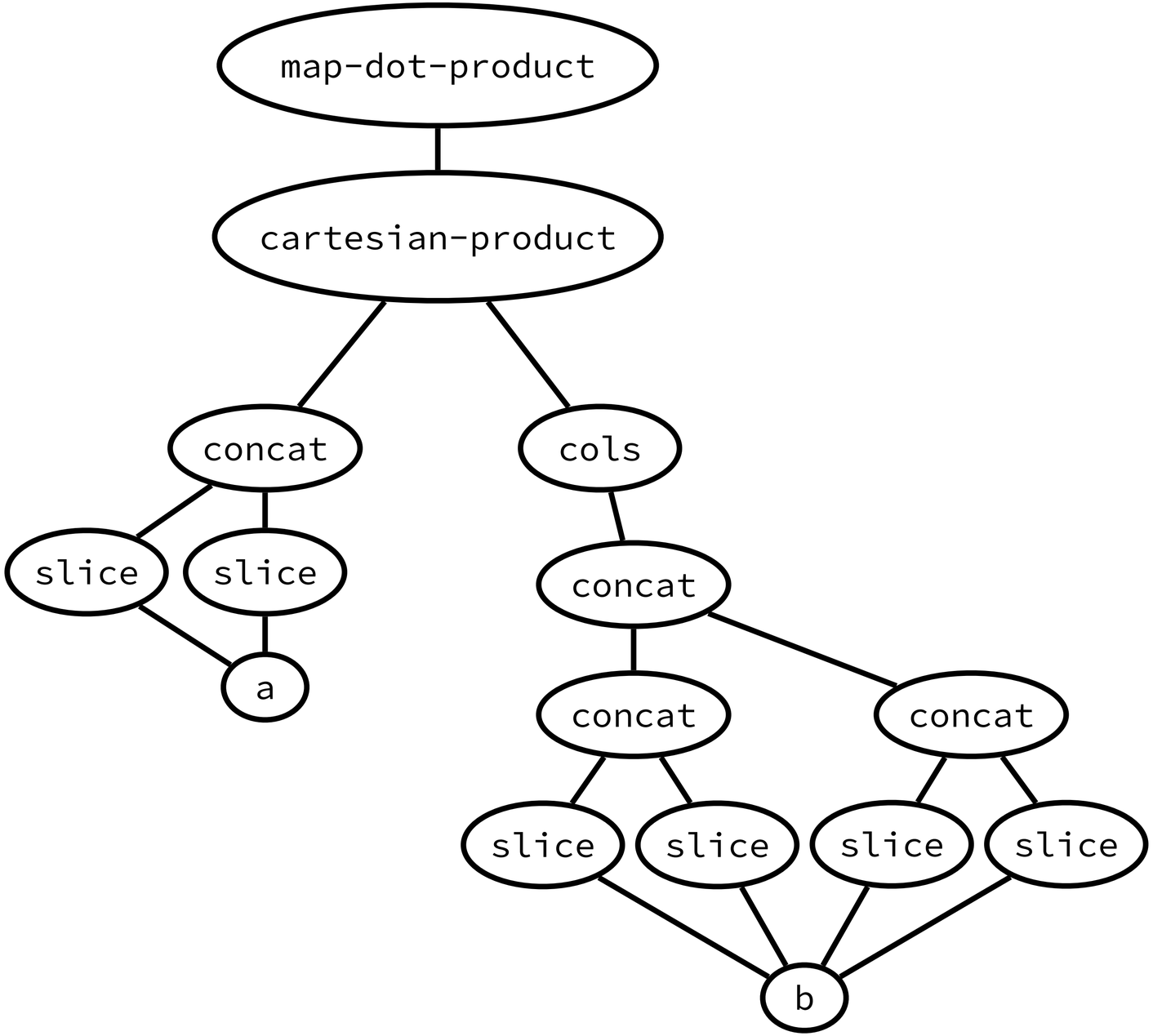

map-dot-product
cartesian-product
a
cols
b


map-dot-product
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concat
cols
slice
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concat
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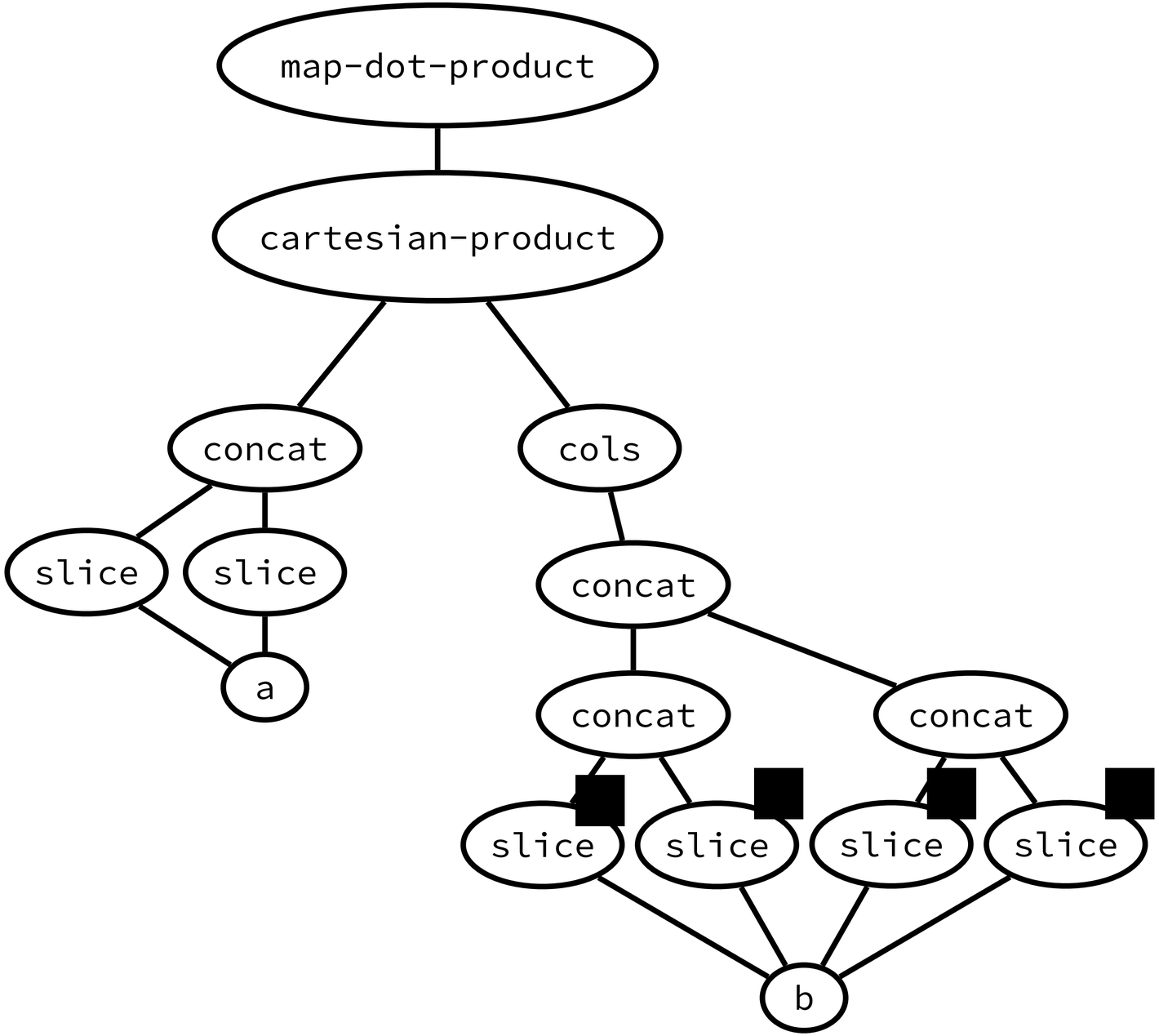
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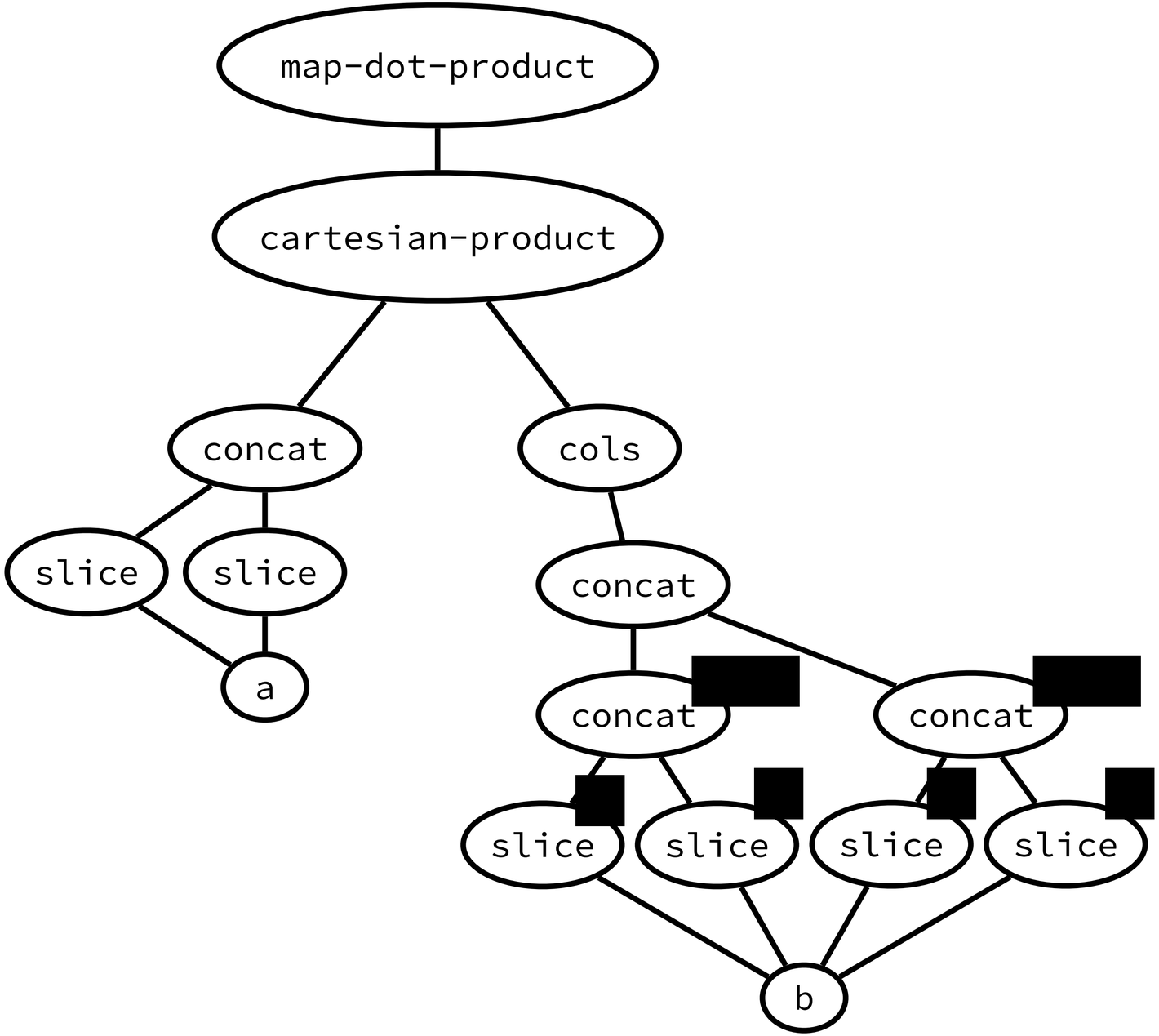
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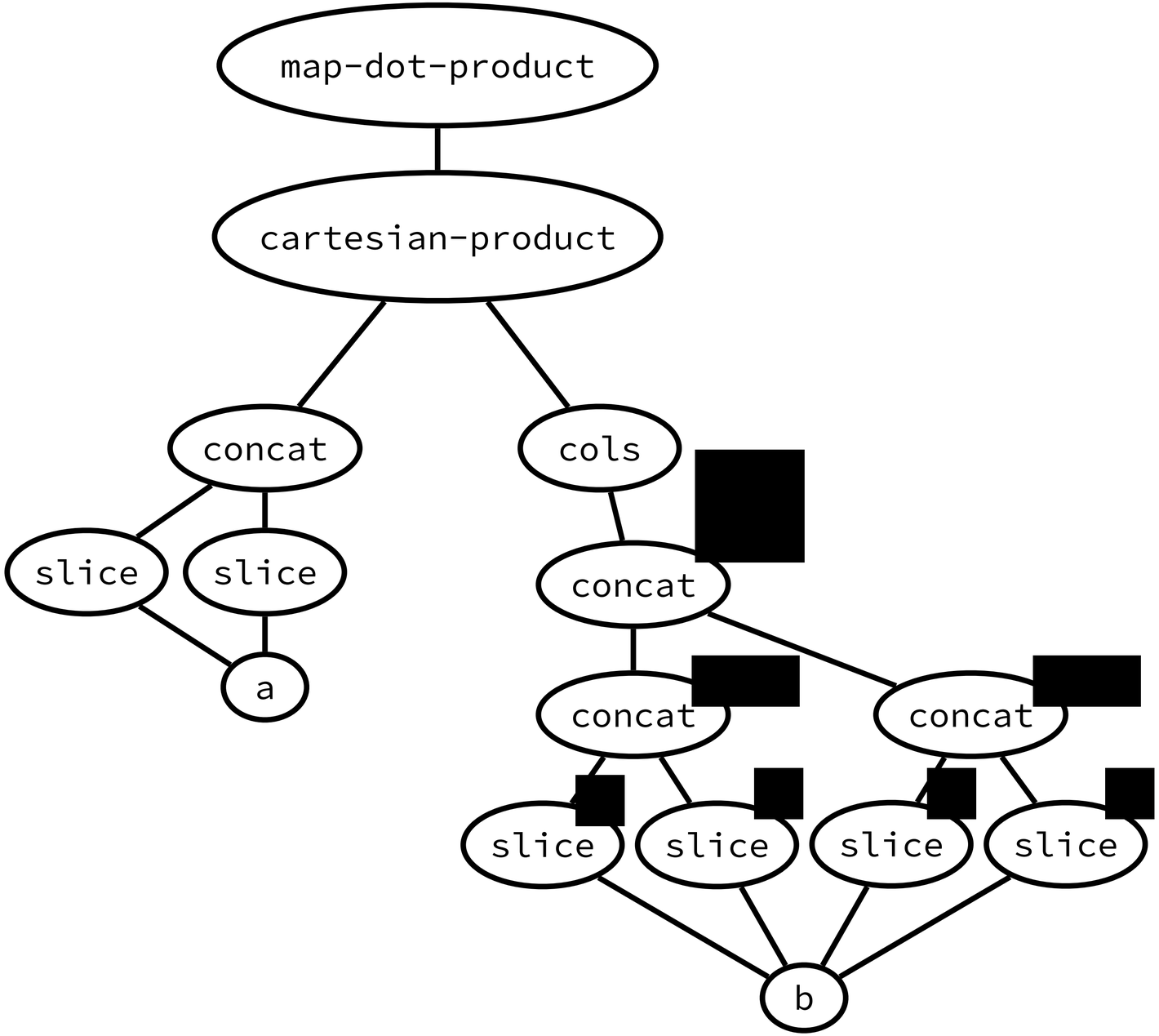
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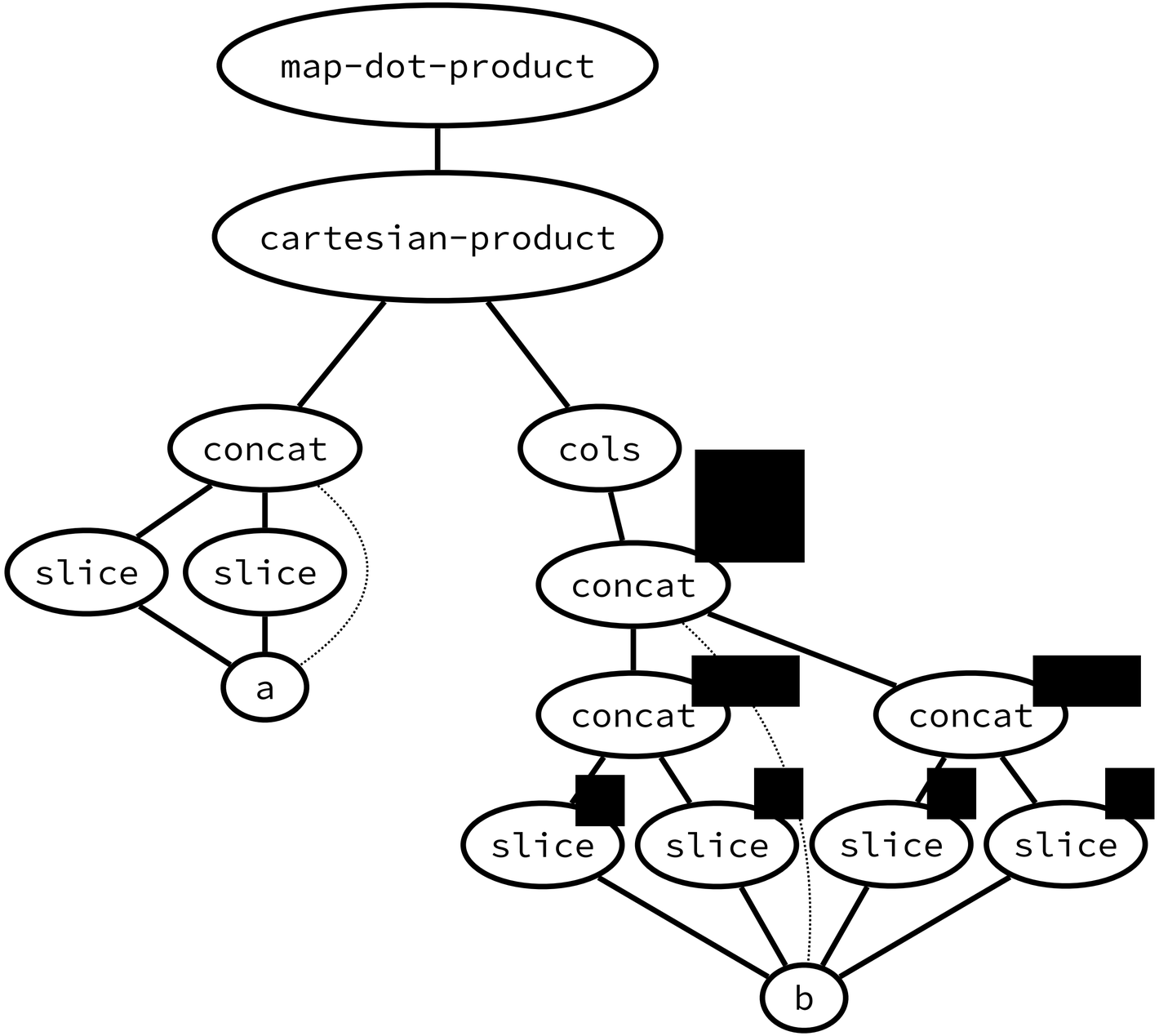
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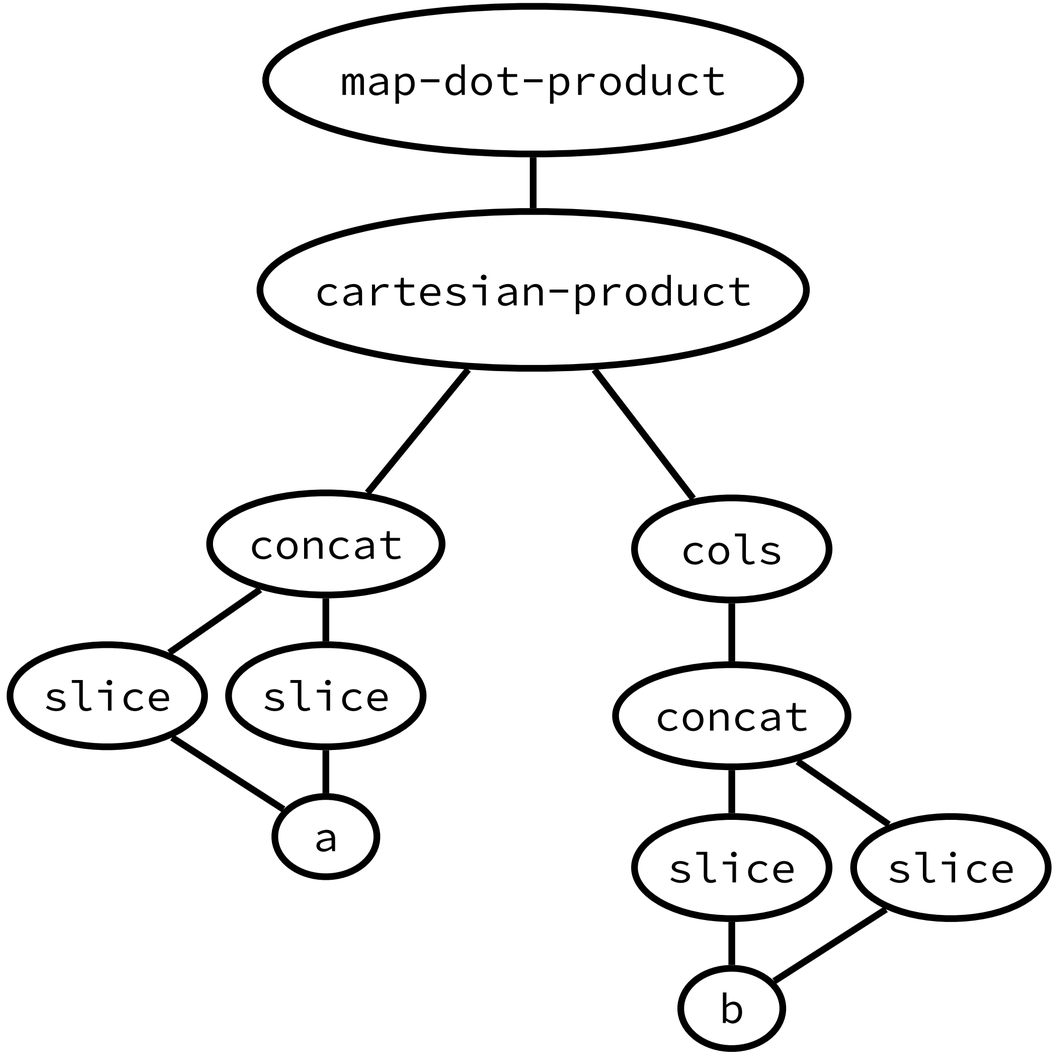
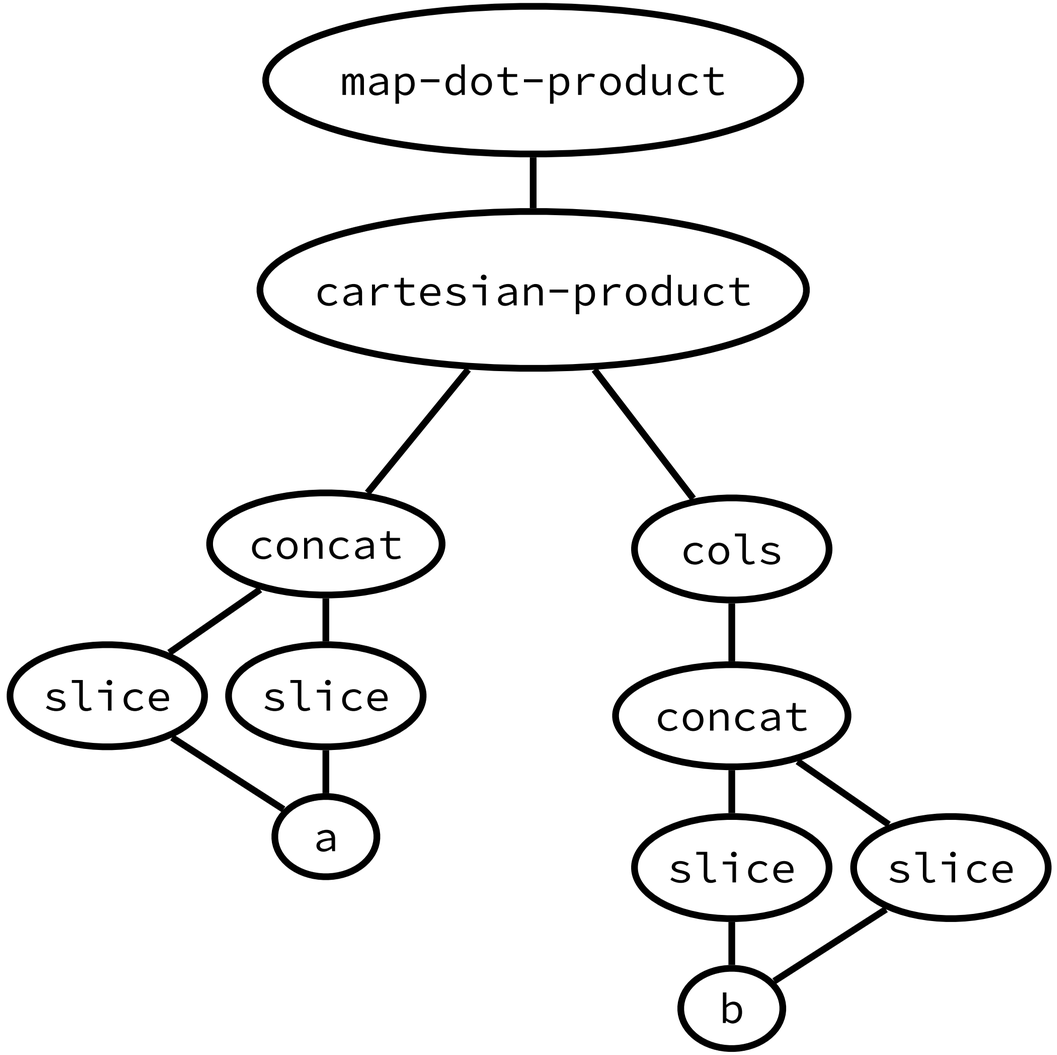


(let’s keep this graph simple!)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concat
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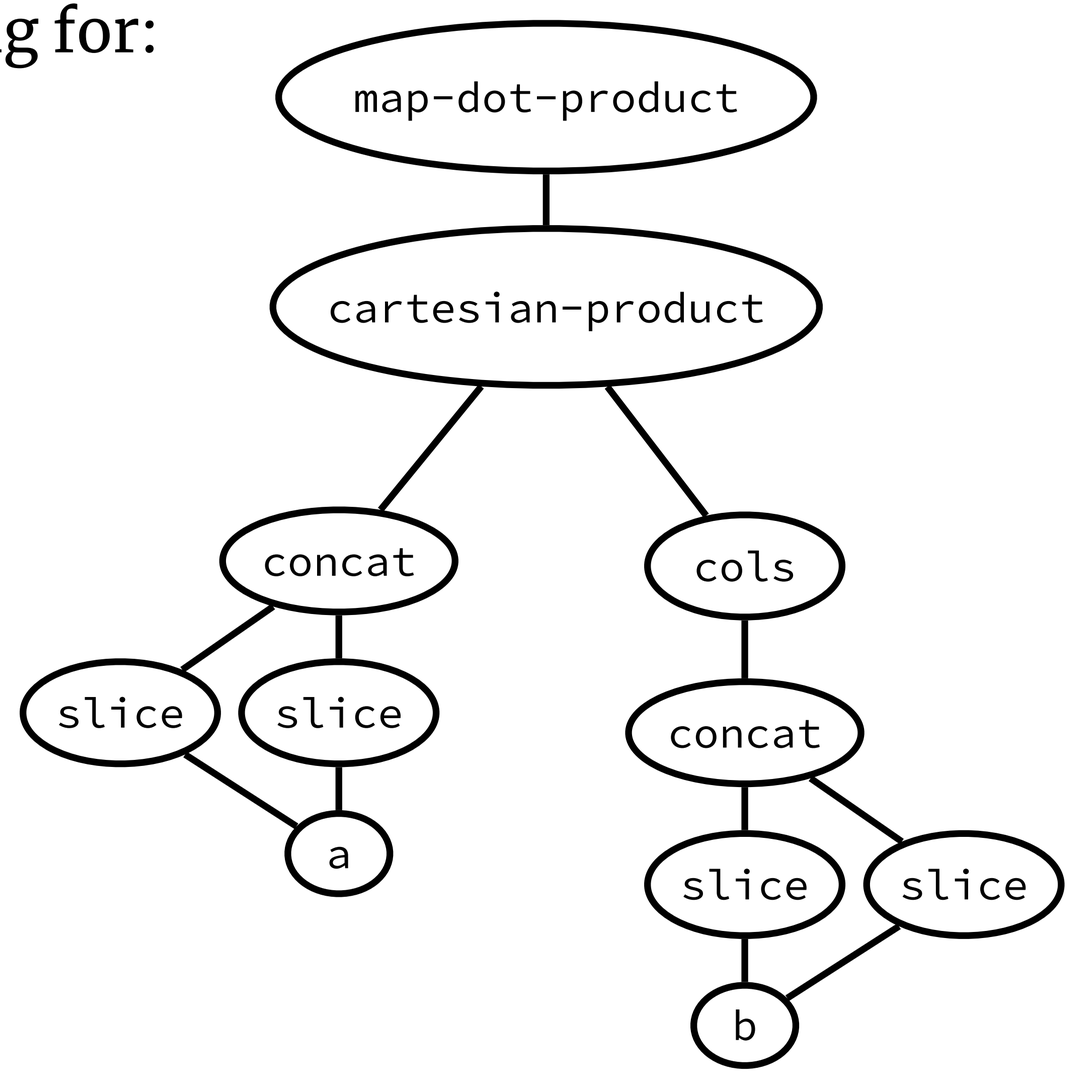
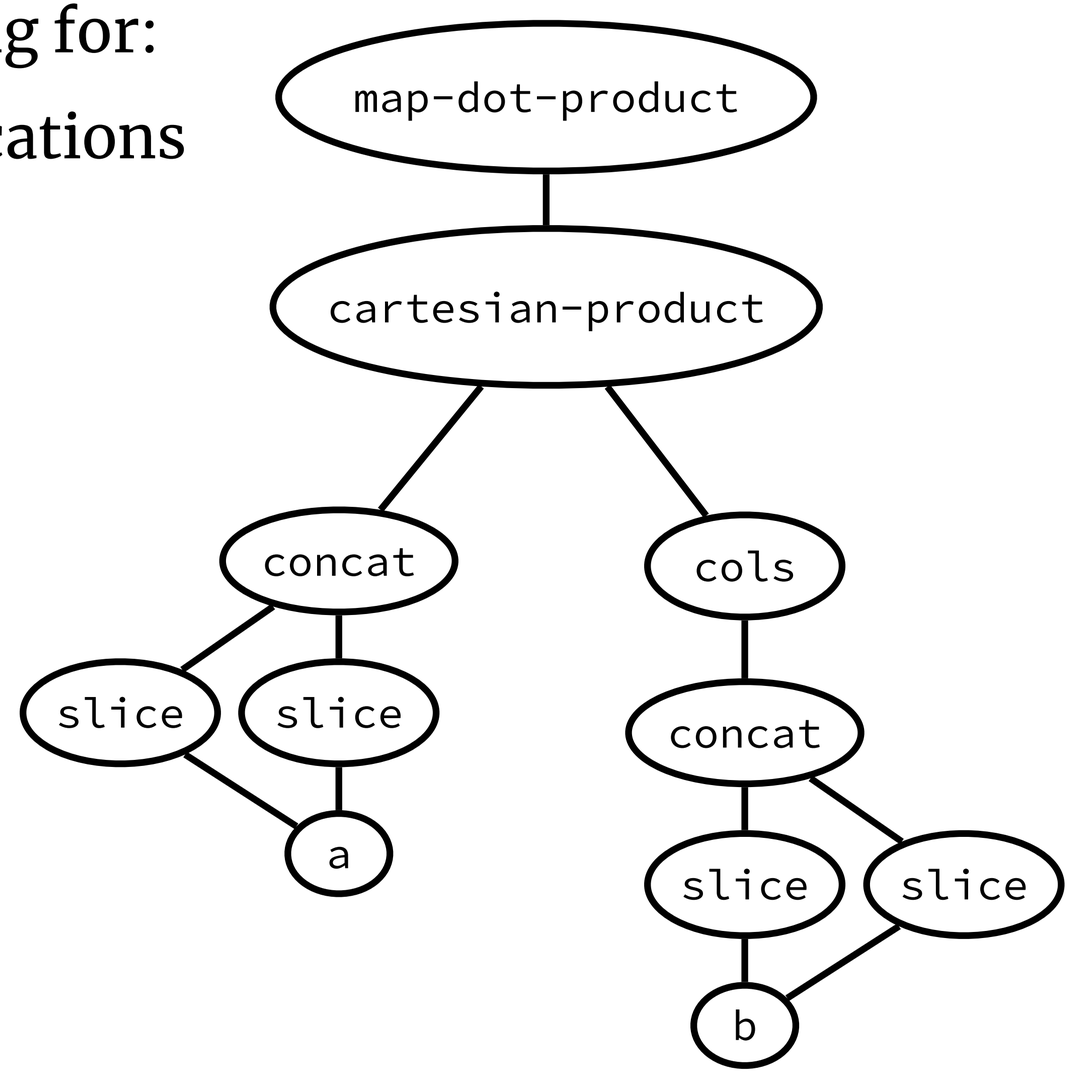


Recall what we're looking for:

Vector–matrix multiplications of different sizes!



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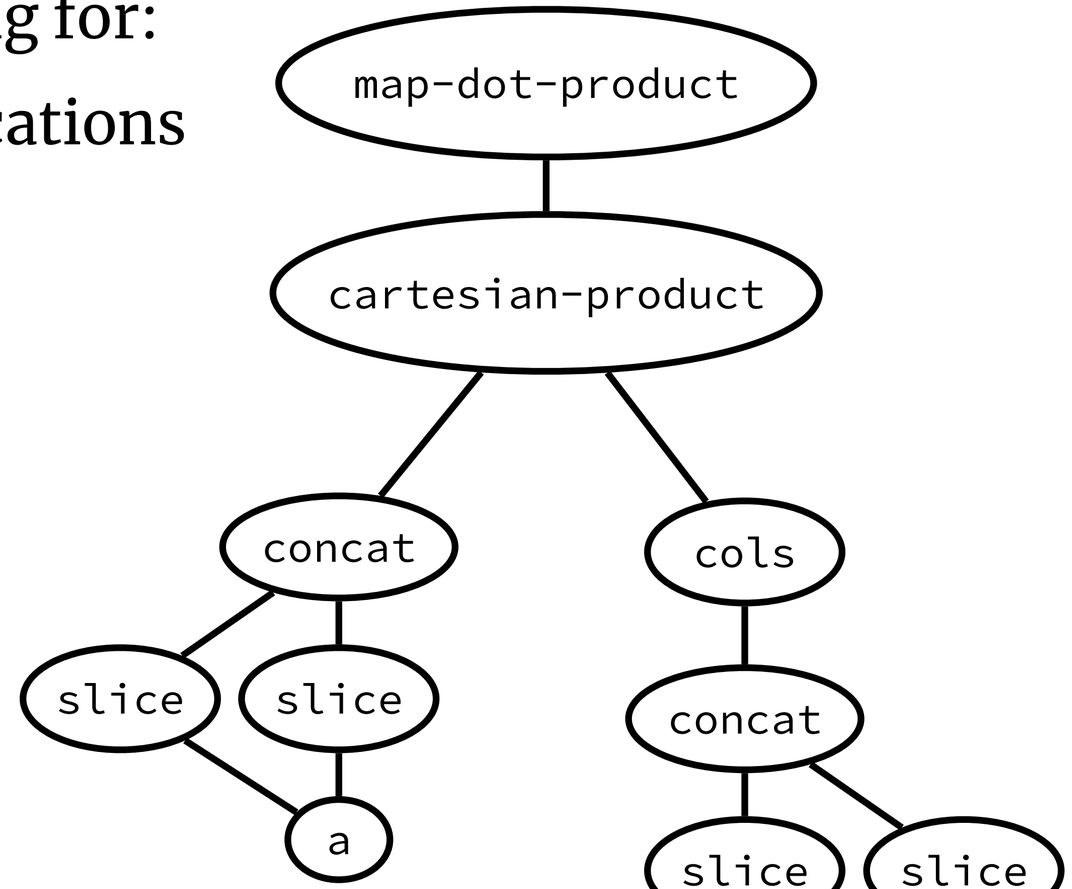

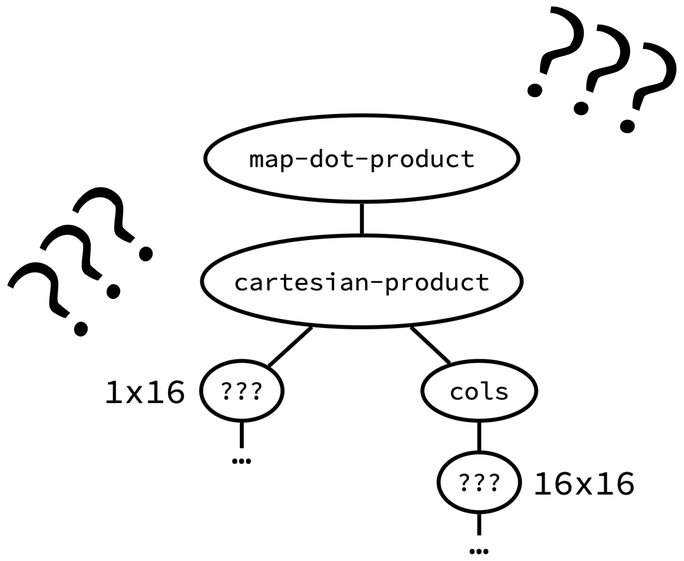

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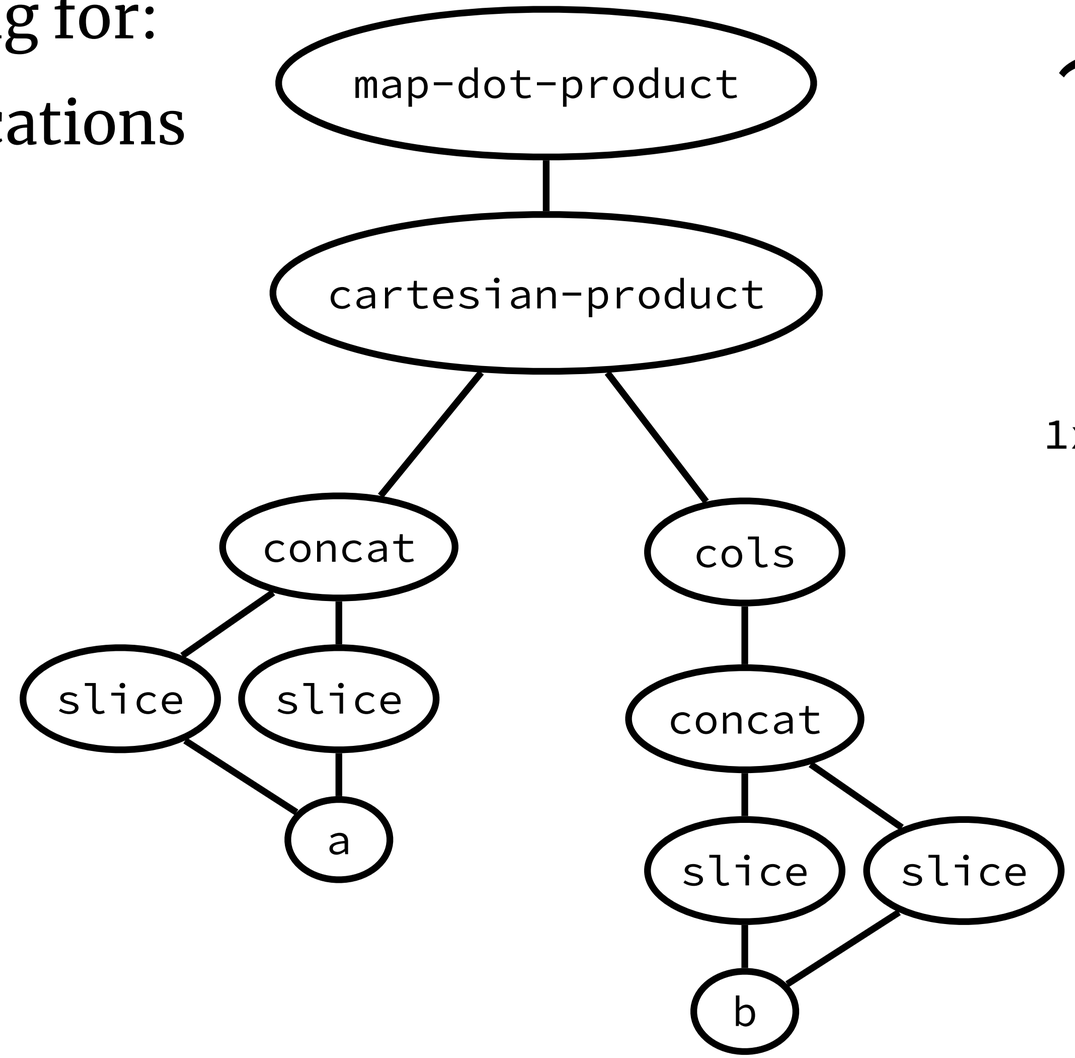

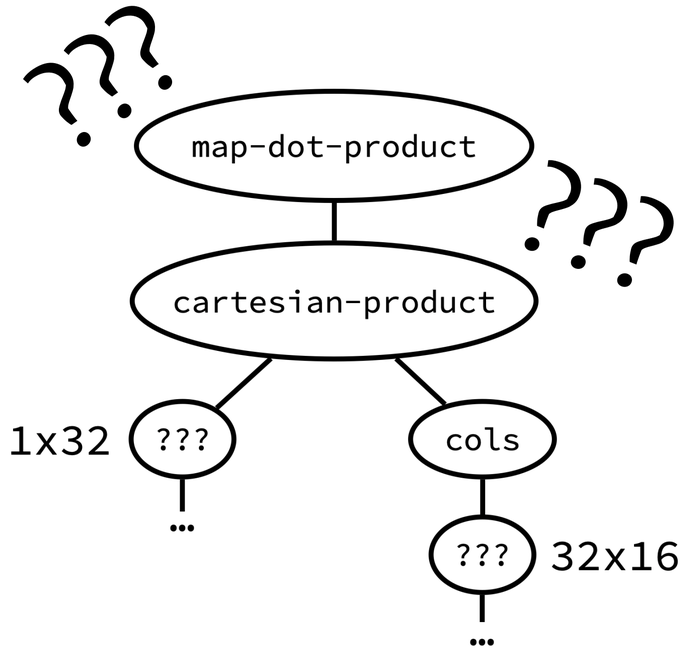

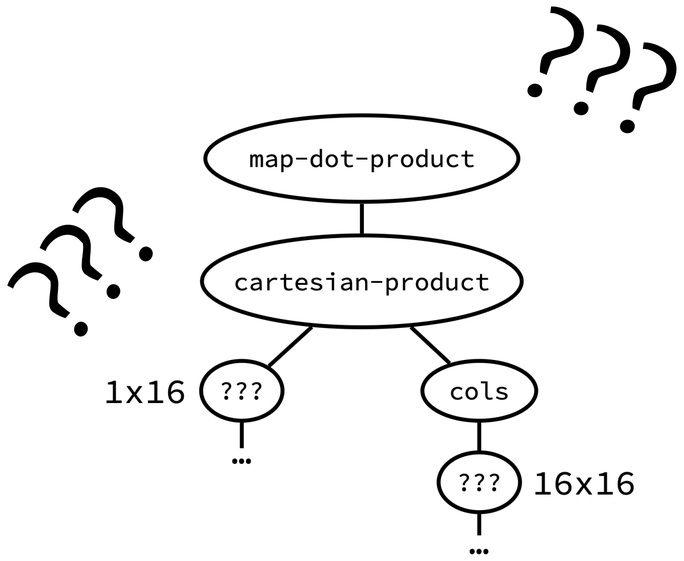

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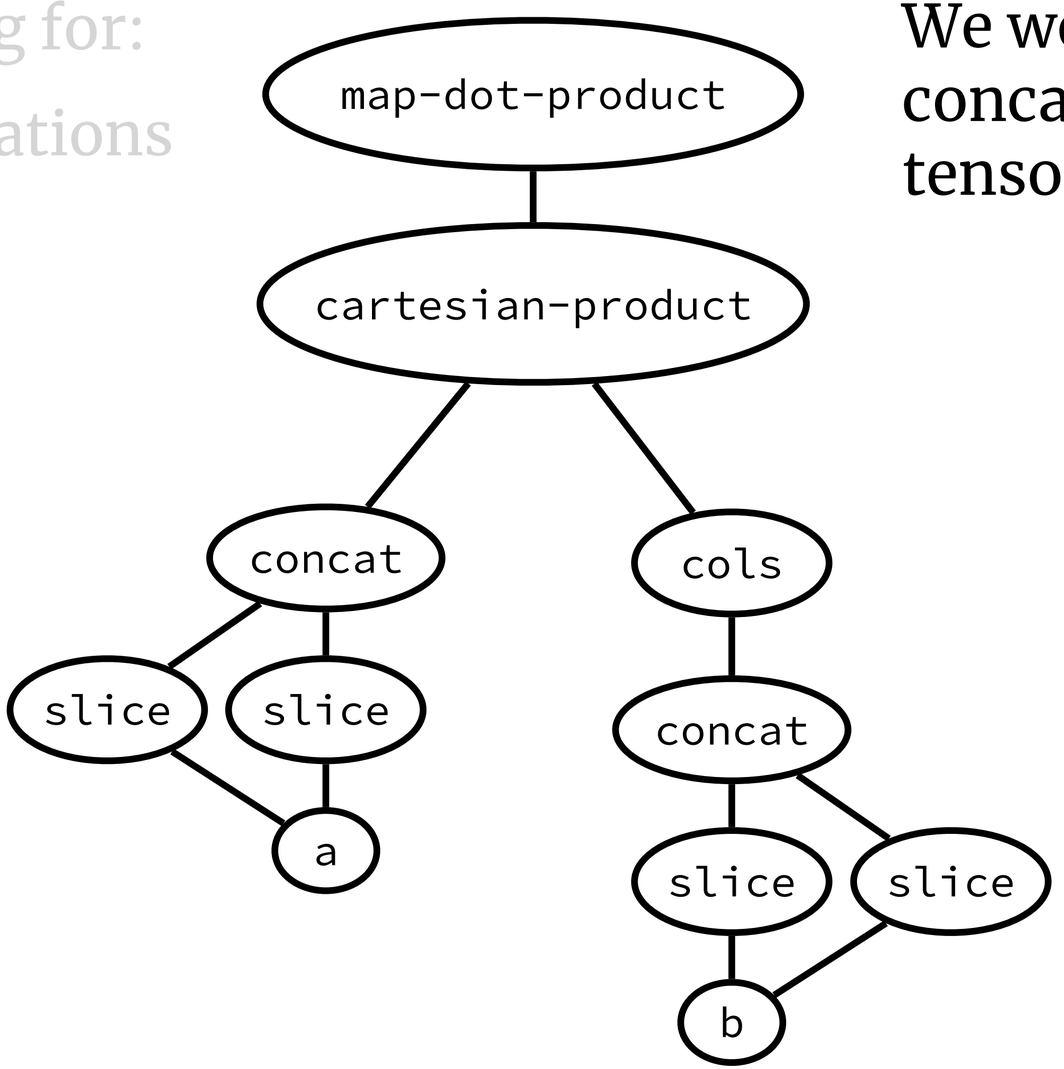

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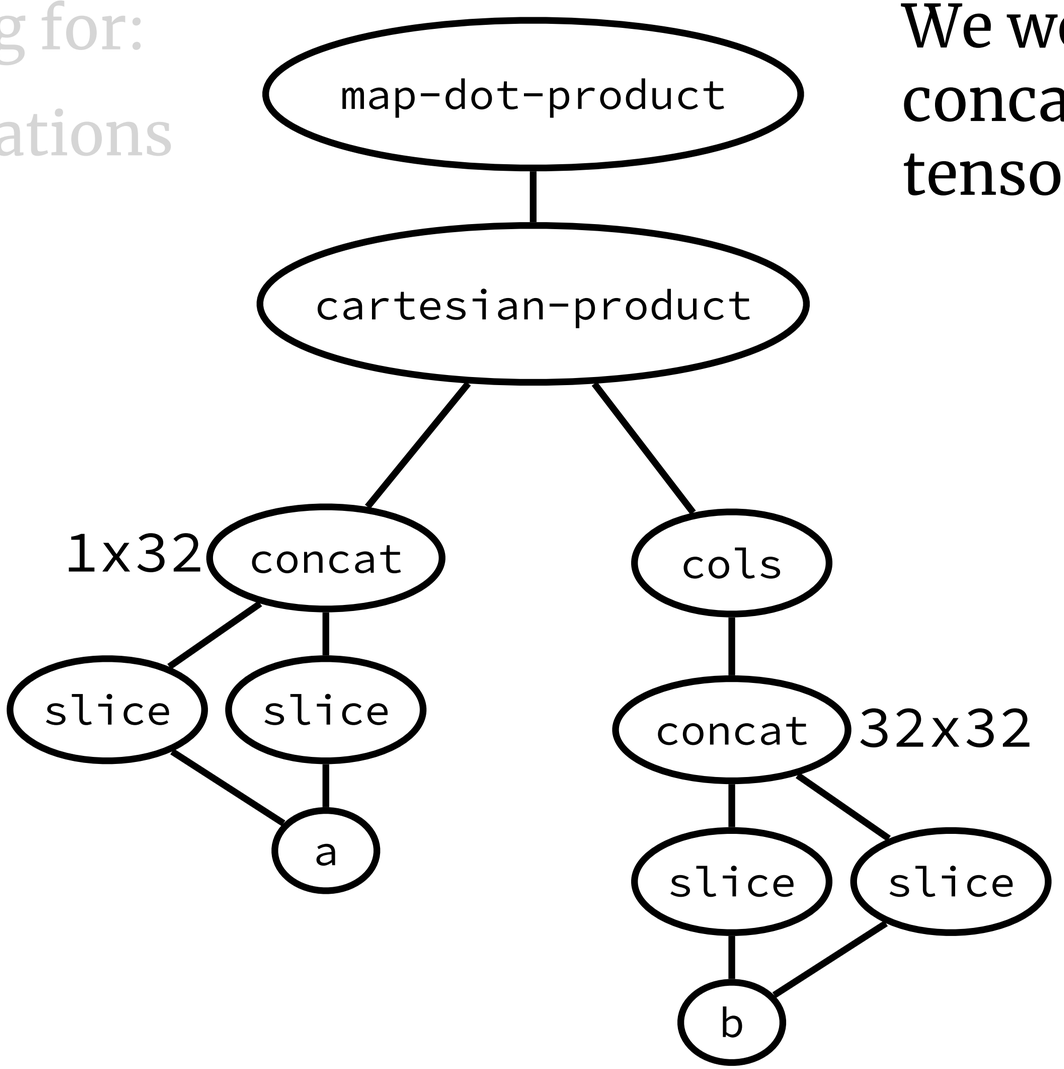

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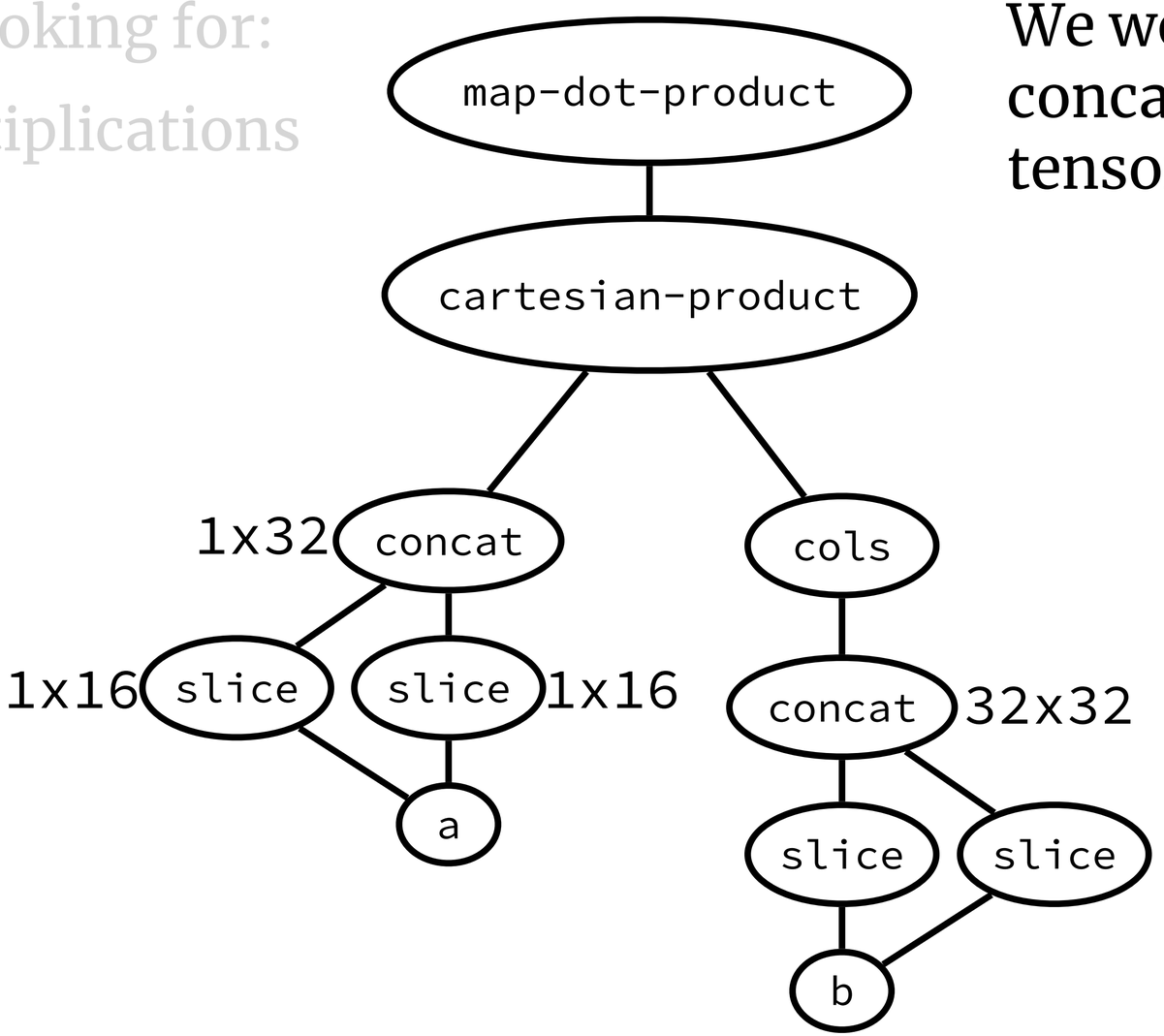

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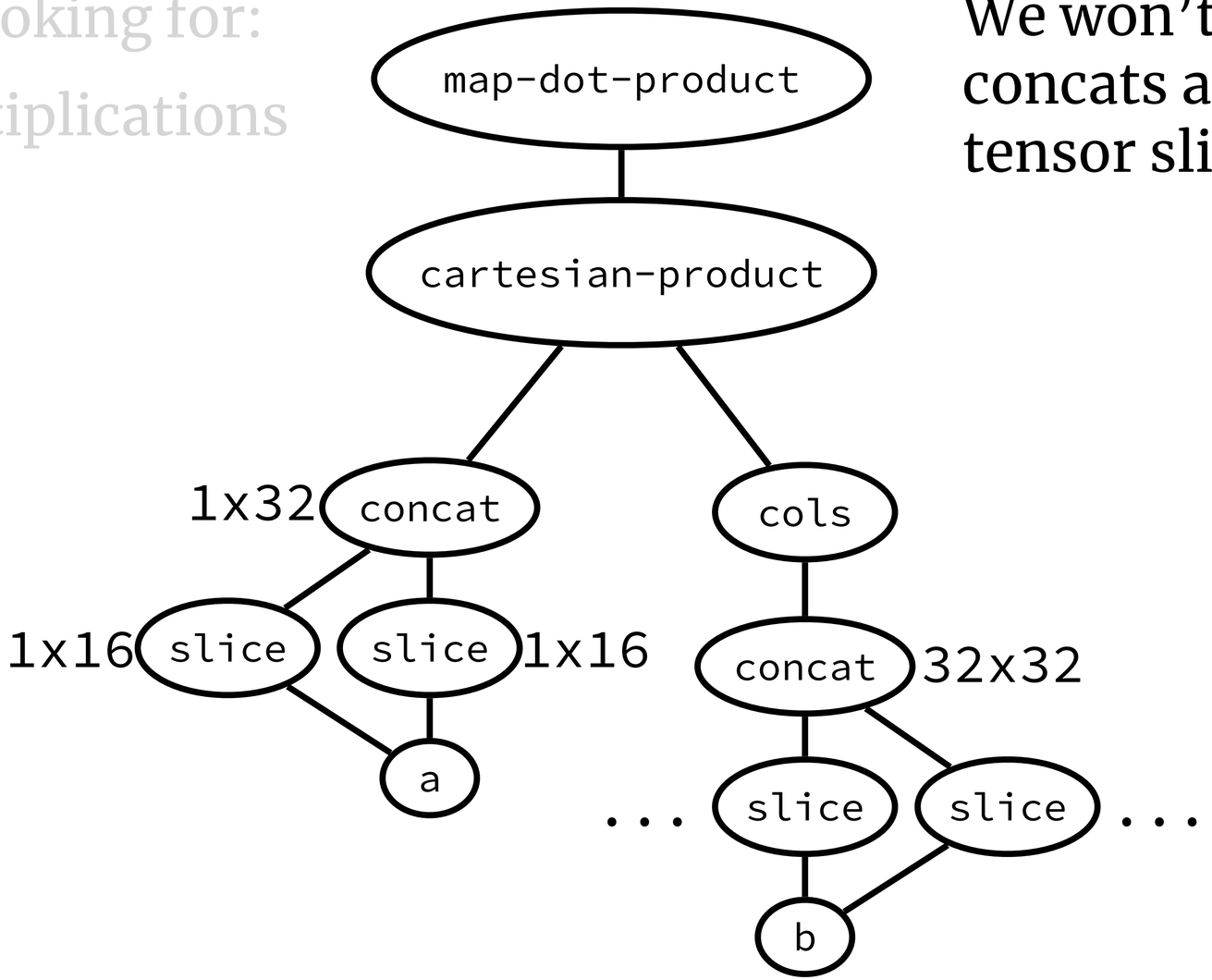

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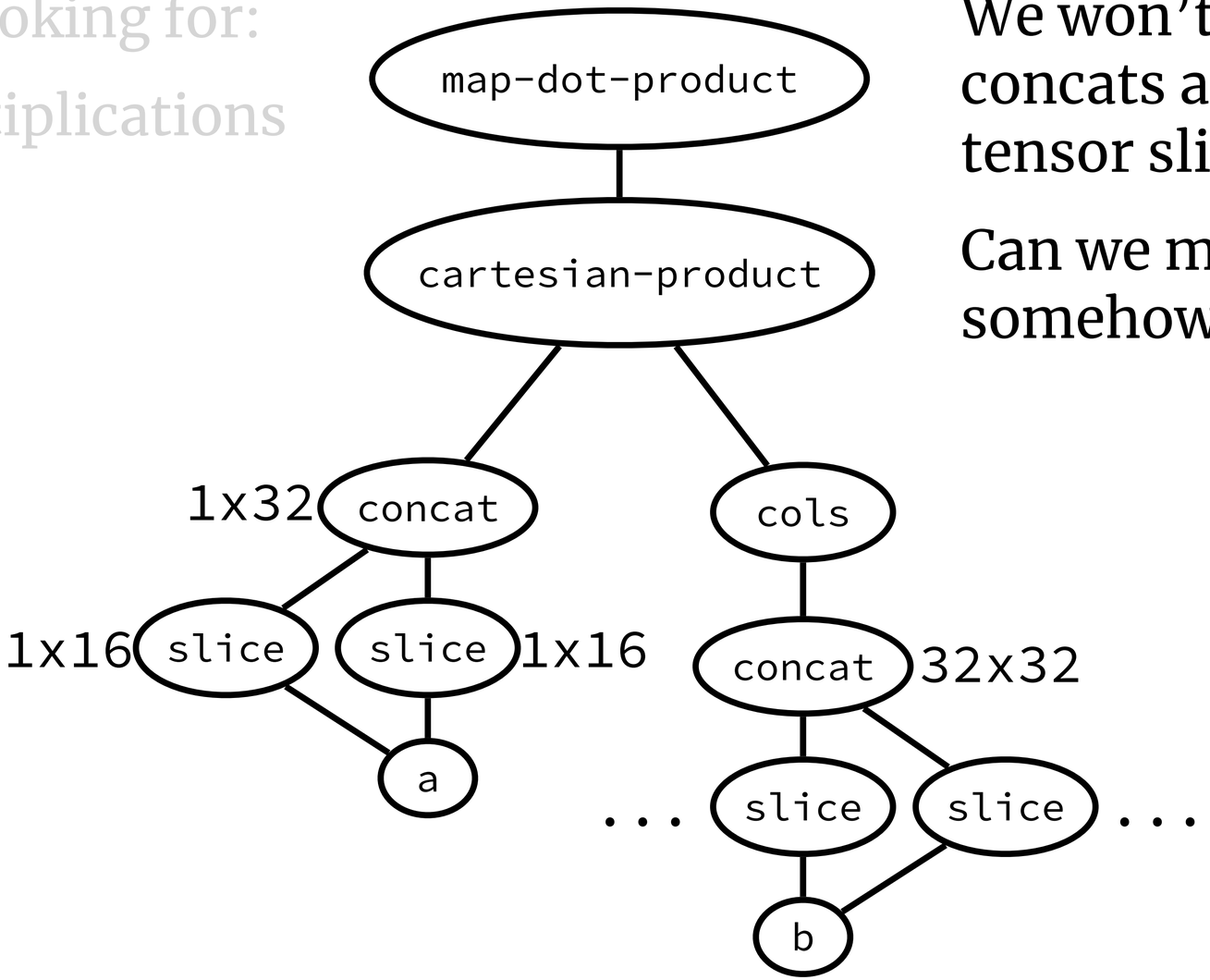

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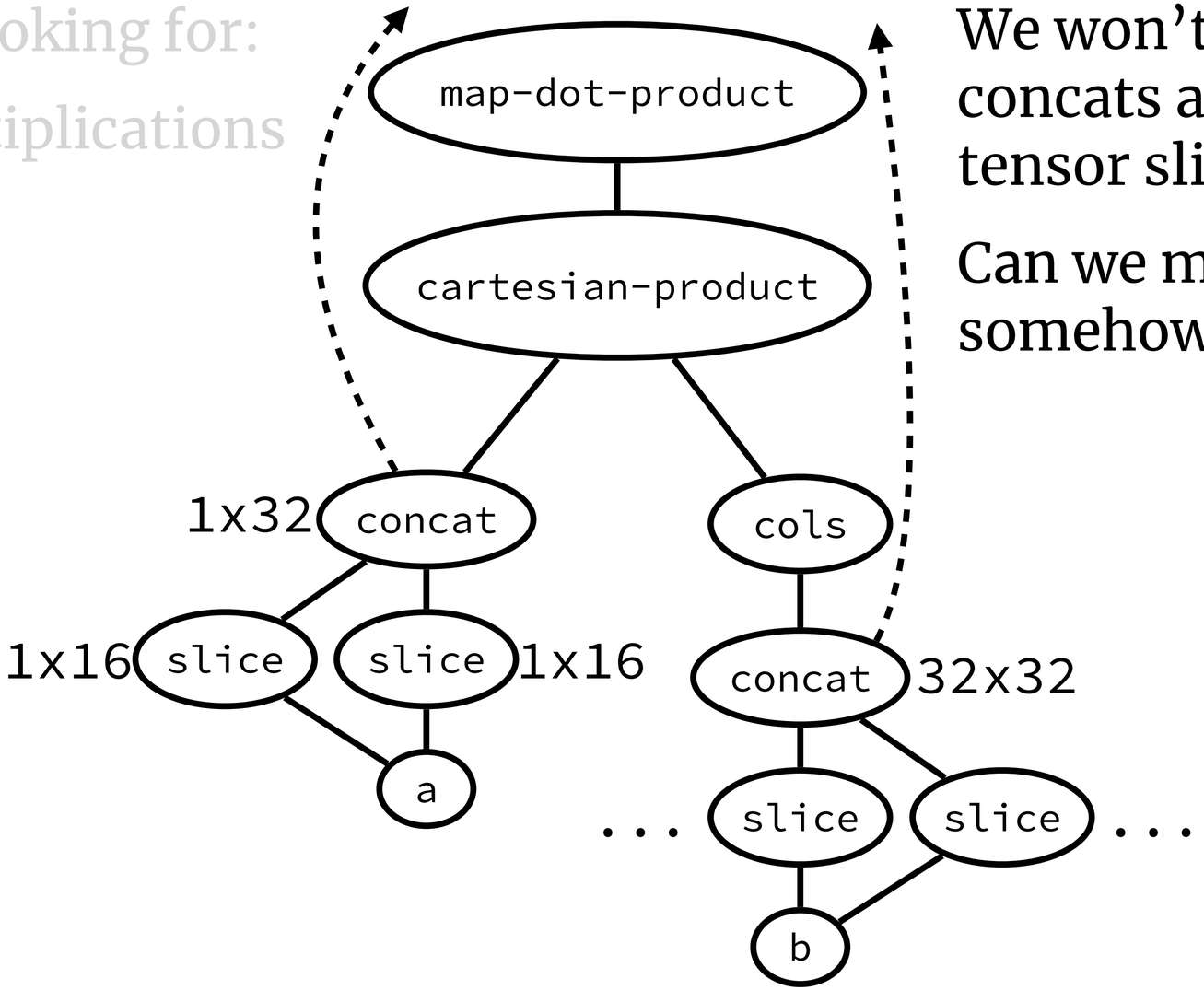

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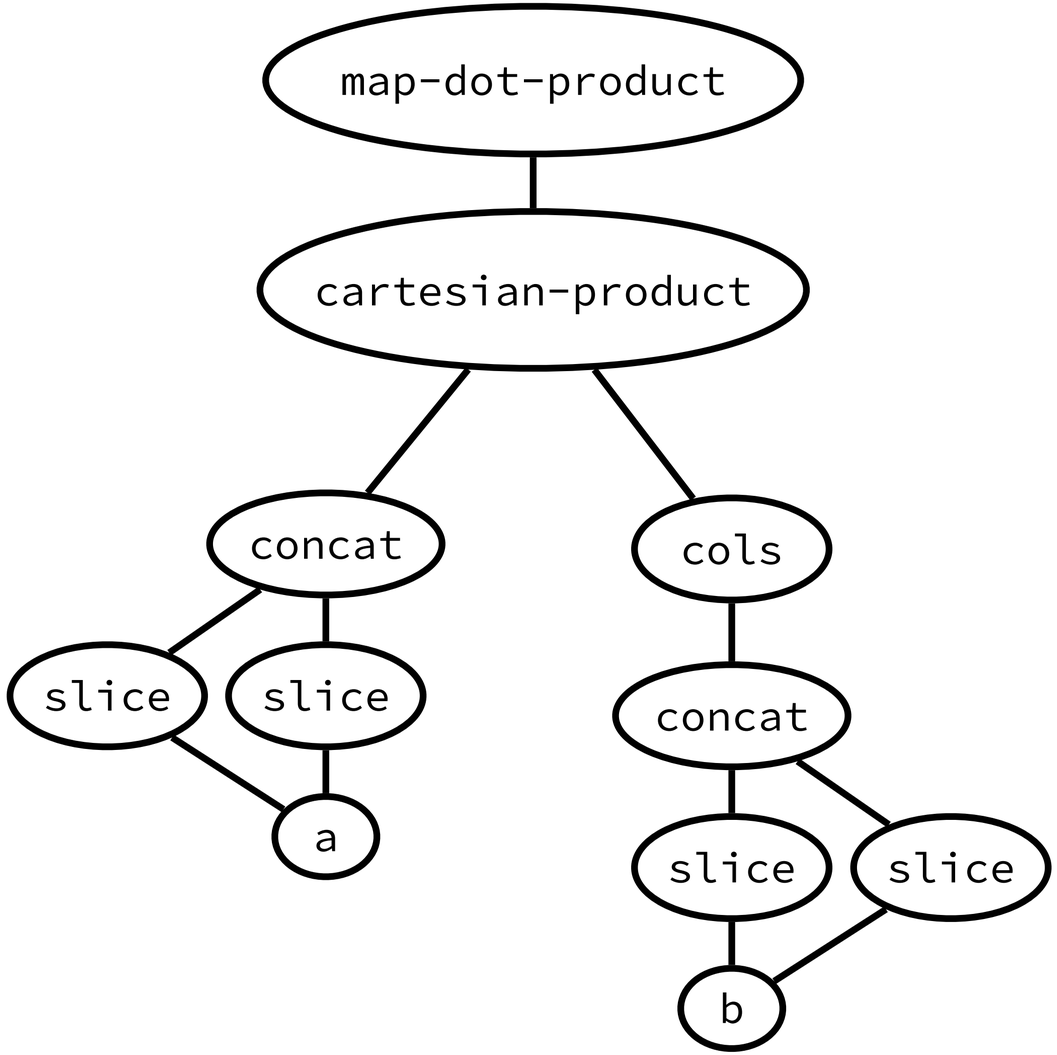
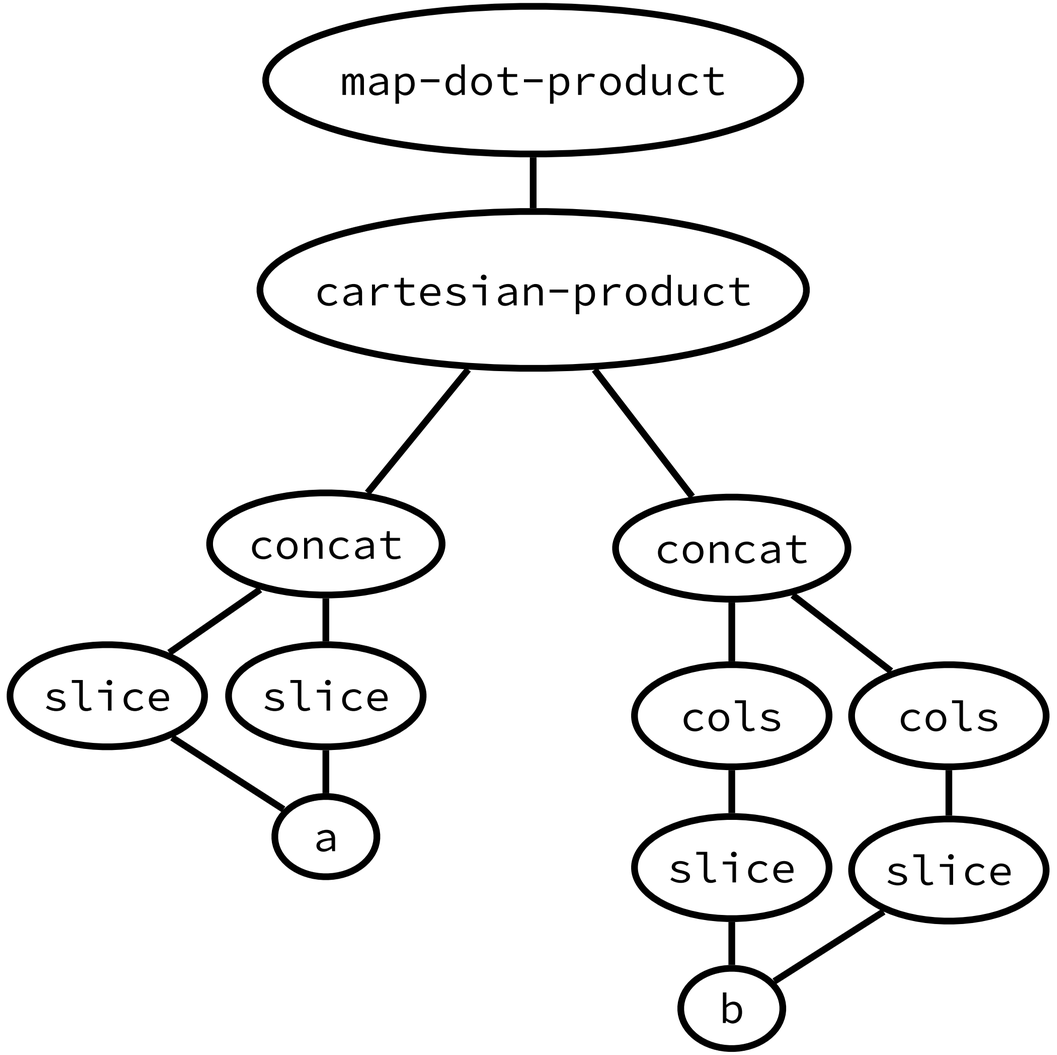
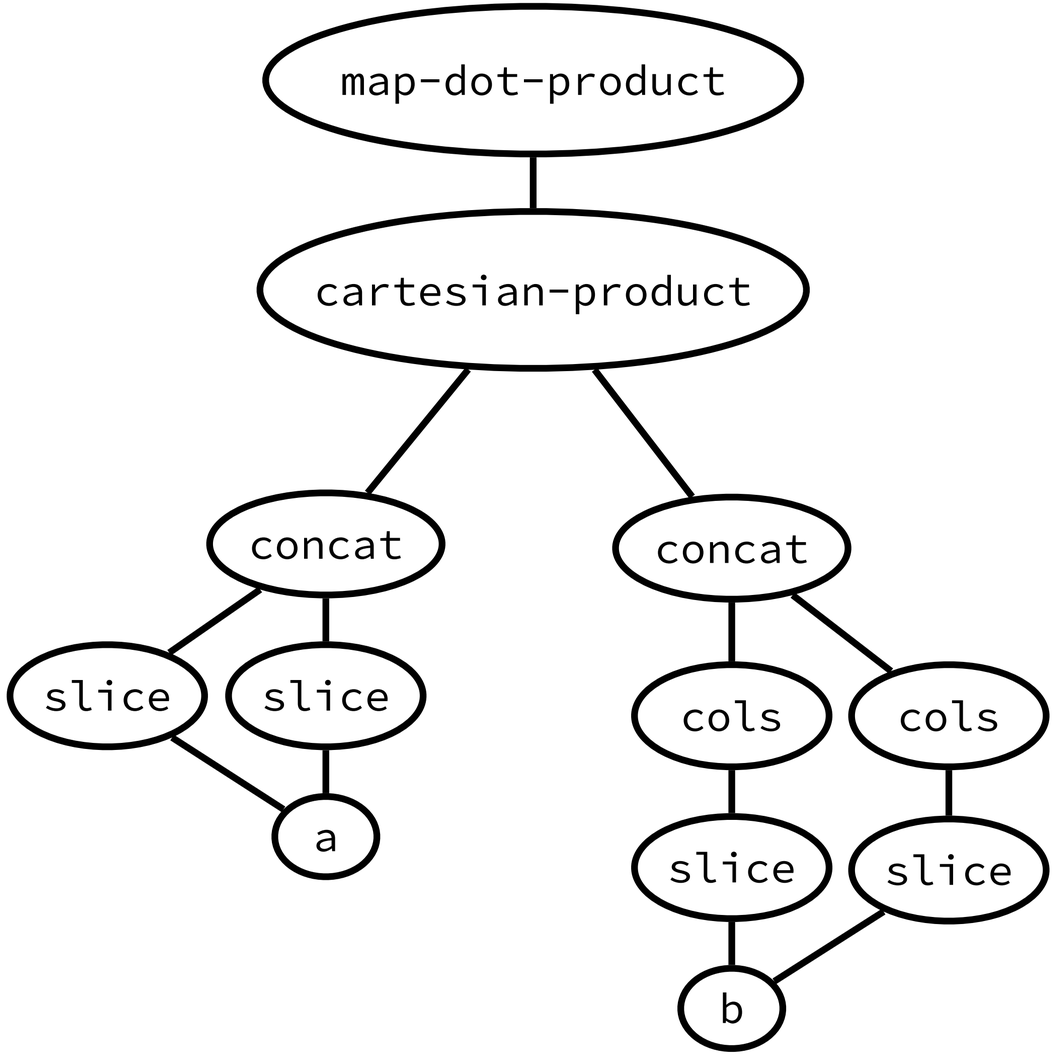
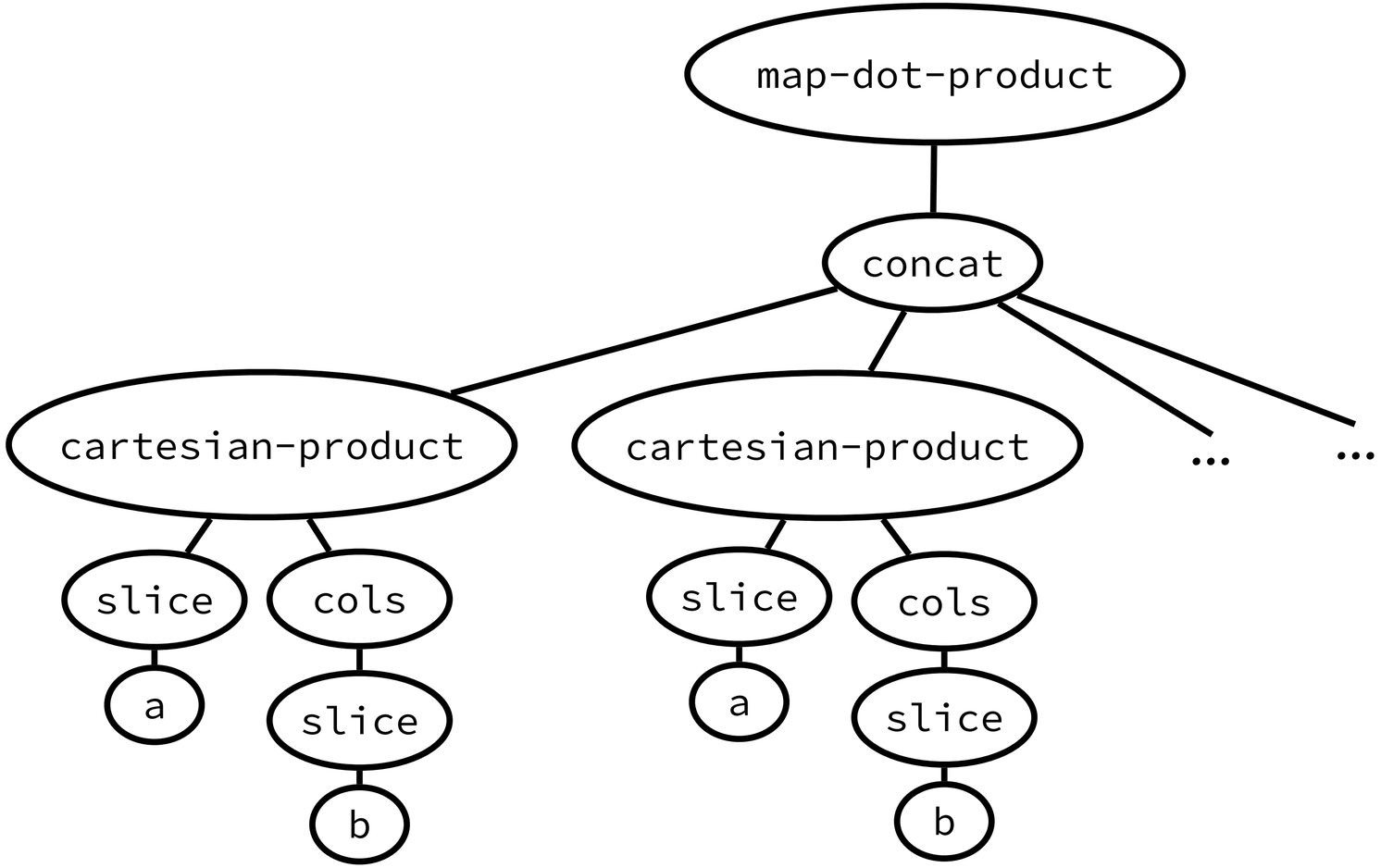
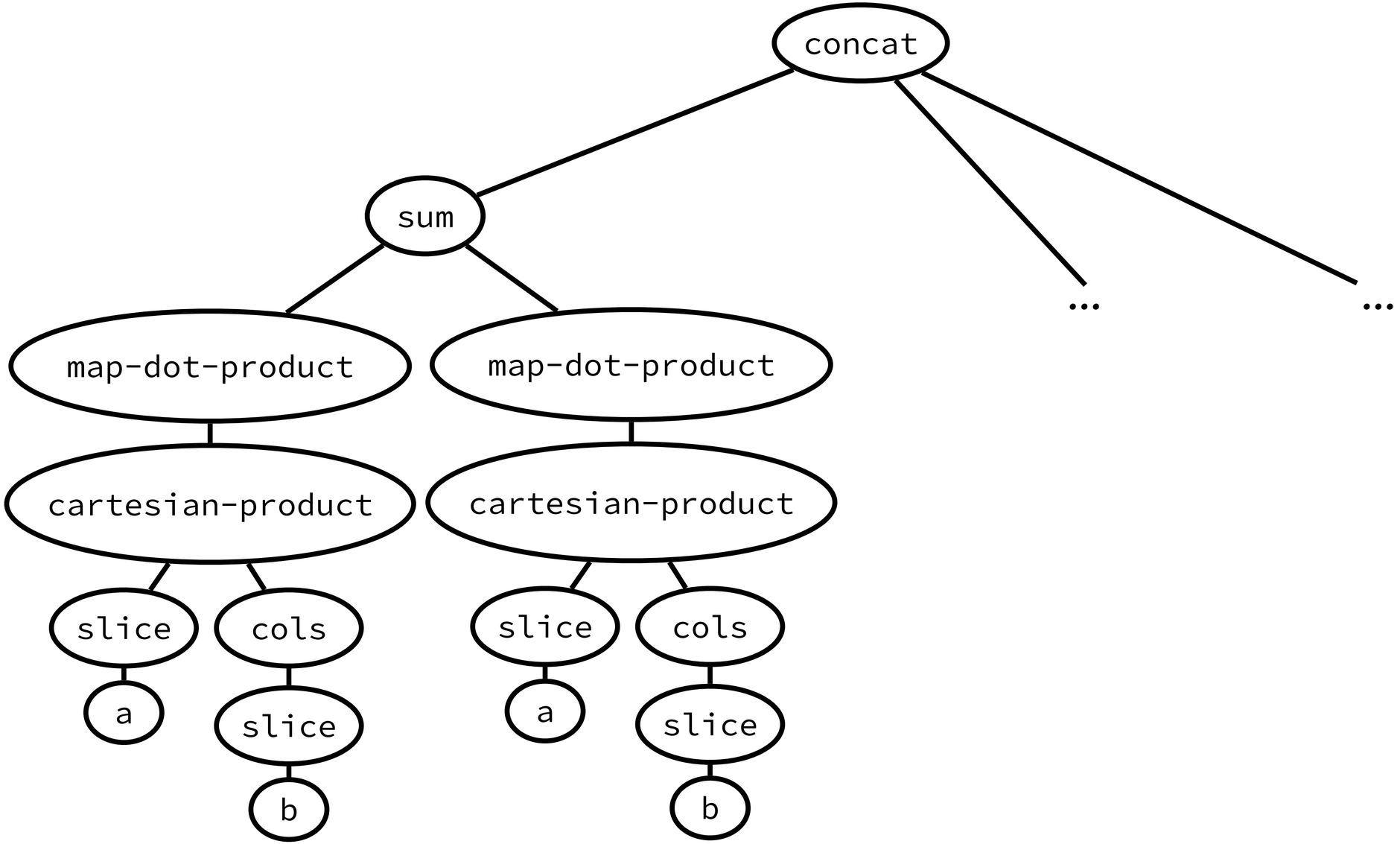

map-dot-product
cartesian-product
concat
cols
slice
slice
concat
a
slice
slice
b

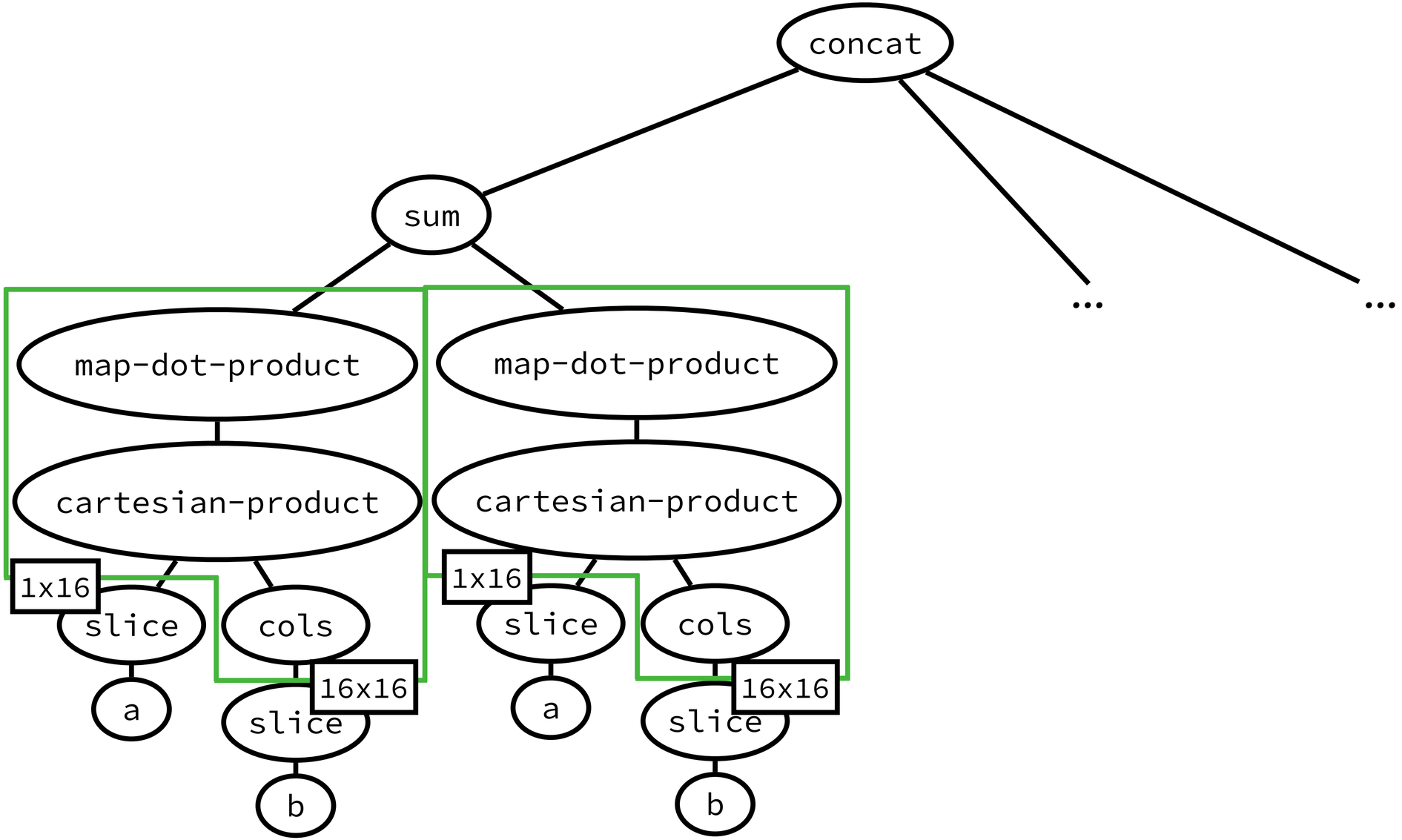


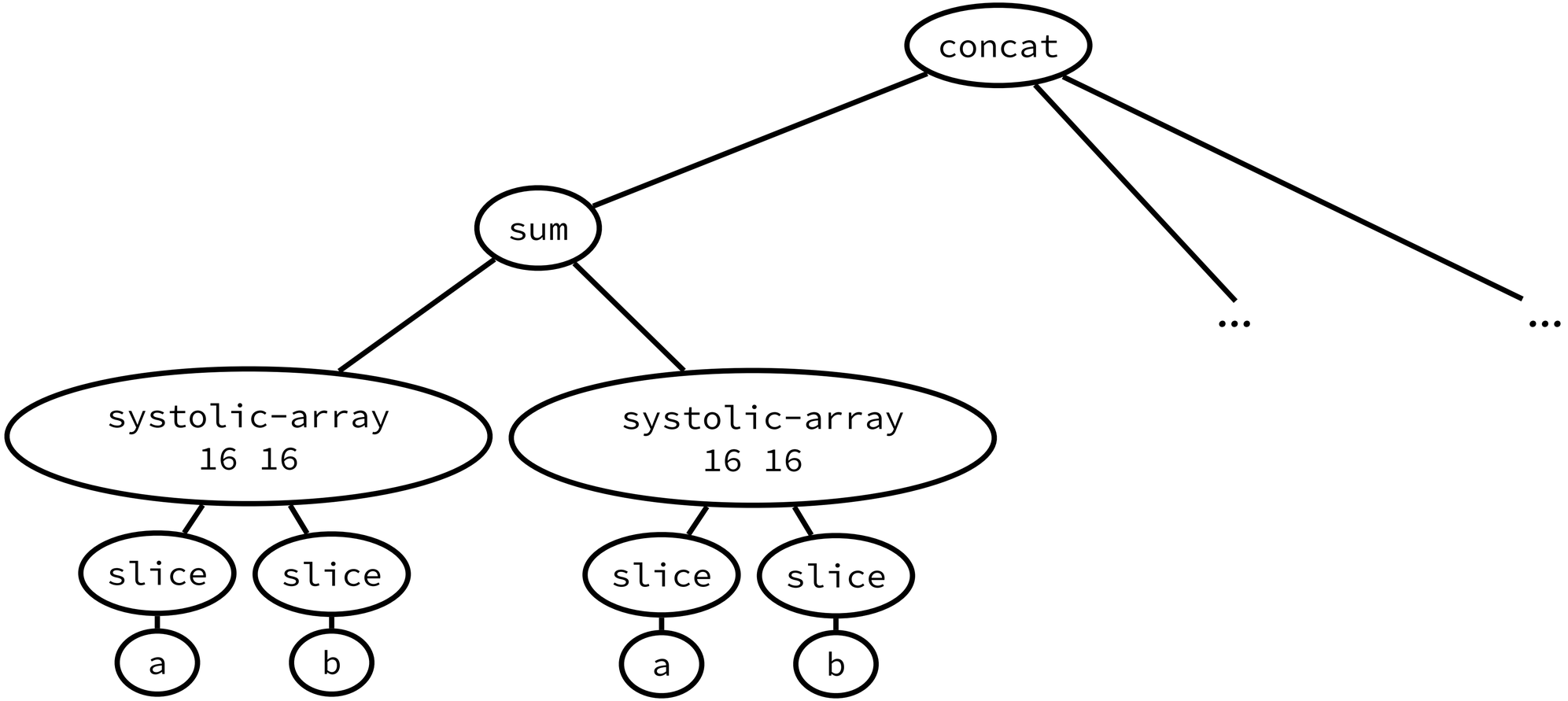

```
egg::rewrite!("bubble-concat-through-cols";
              "(cols (concat a b))"
              => "(concat (cols a) (cols b))")
```

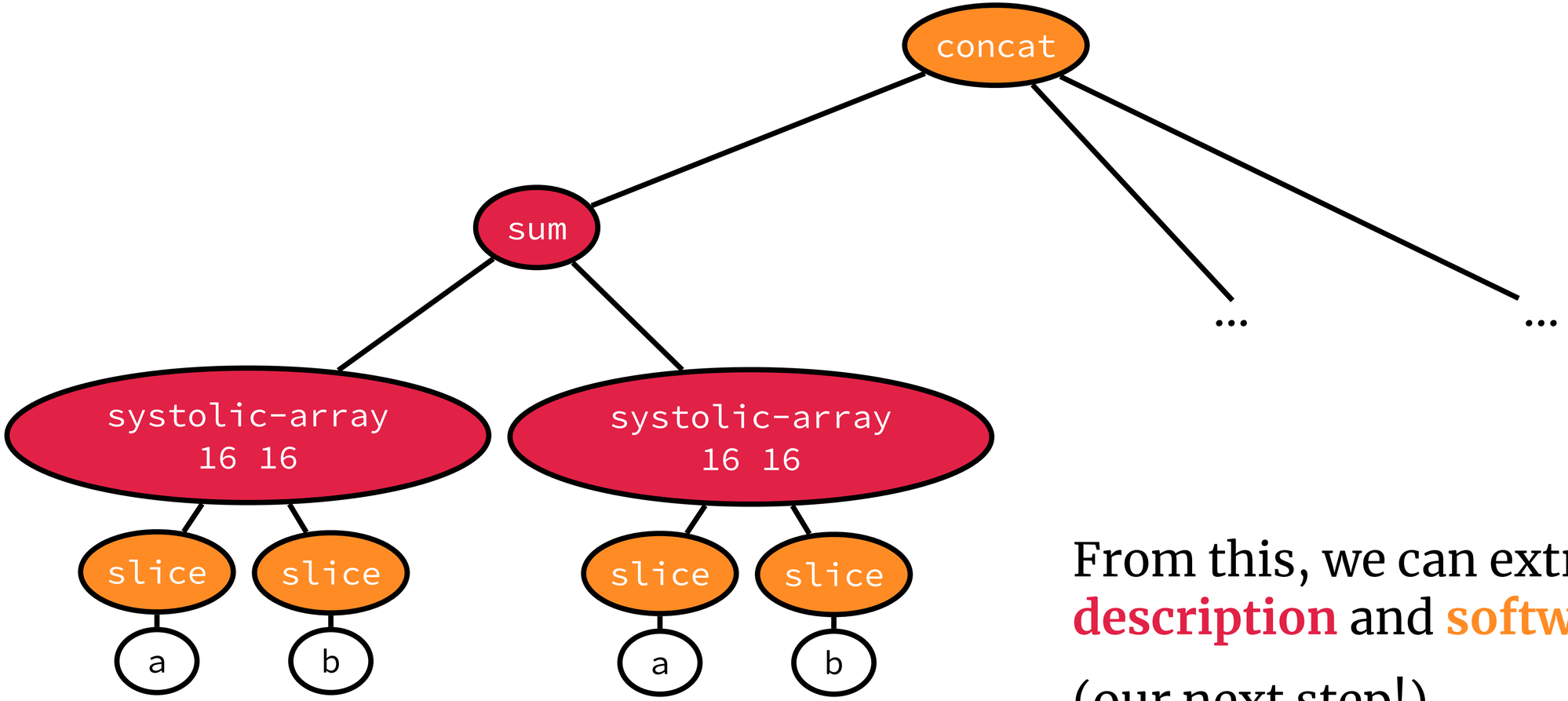

map-dot-product
cartesian-product
concat
concat
slice
slice
cols
cols
a
slice
slice
b


map-dot-product
concat
cartesian-product
cartesian-product
...
...
slice
cols
slice
cols
a
slice
a
slice
b
b


concat
sum
...
...
map-dot-product
map-dot-product
cartesian-product
cartesian-product
slice
cols
slice
cols
a
slice
a
slice
b
b


concat
sum
...
...
map-dot-product
map-dot-product
cartesian-product
cartesian-product
1x16
1x16
slice
cols
slice
cols
16x16
16x16
a
a
slice
slice
b
b


concat
sum
...
...
systolic-array
16 16
systolic-array
16 16
slice
slice
slice
slice
a
b
a
b



From this, we can extract a **hardware description** and **software schedule**.

(our next step!)

Early Results

Early Results

```
let program = "
 (map-dot-product
  (cartesian-product
   v-32
   (cols t-32-32)
  )
 )
 "
.parse()
.unwrap();
```

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   (cols t-32-32)
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```

```
let rws = vec![
    rewrites::split(0, 16, true),
    rewrites::split(1, 16, true),
    rewrites::collapse_nested_slices(),
    rewrites::bubble_concat_through_rows_axis_0(),
    rewrites::bubble_concat_through_rows_axis_1(),
    rewrites::bubble_concat_through_cols_axis_0(),
    rewrites::bubble_concat_through_cols_axis_1(),
    rewrites::bubble_concat_through_cartesian_product_not_last_axis_left(),
    rewrites::bubble_concat_through_cartesian_product_not_last_axis_right(),
    rewrites::bubble_concat_through_cartesian_product_last_axis(),
    rewrites::bubble_concat_through_map_dot_product_not_last_axis(),
    rewrites::bubble_concat_through_map_dot_product_last_axis(),
    rewrites::systolic_array_vector_matrix(),
];
```

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    rewrites::bubble_concat_through_cols_axis_0(),
    rewrites::bubble_concat_through_cols_axis_1(),
    rewrites::bubble_concat_through_cartesian_product_not_last_axis_left(),
    rewrites::bubble_concat_through_cartesian_product_not_last_axis_right(),
    rewrites::bubble_concat_through_cartesian_product_last_axis(),
    rewrites::bubble_concat_through_map_dot_product_not_last_axis(),
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];
```

```
let (egraph, id) = egg::EGraph::<Language, Meta>::from_expr(&program);
let runner = egg::Runner::new().with_egraph(egraph).run(&rws);
```

```
"(concat
  (elementwise-add
   (bsg-systolic-array 16 16
    (slice v-32 0 16)
    (slice t-32-32 0 16 0 16)
   )
   (bsg-systolic-array 16 16
    (slice v-32 16 32)
    (slice t-32-32 16 32 0 16)
   )
  )
  (elementwise-add
   (bsg-systolic-array 16 16
    (slice v-32 0 16)
    (slice t-32-32 0 16 16 32)
   )
   (bsg-systolic-array 16 16
    (slice v-32 16 32)
    (slice t-32-32 16 32 16 32)
   )
  )
  0)"
.parse::<Pattern<_>>()
.unwrap()
.search_eclass(&runner.egraph, id)
.expect("Did not find expected program");
```

```
"(bsg-systolic-array 32 32 v-32 t-32-32)"
    .parse::<Pattern<_>>()
    .unwrap()
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```

```
"(concat
  (bsg-systolic-array 32 16
   v-32
   (slice t-32-32 0 32 0 16)
  )
  (bsg-systolic-array 32 16
   v-32
   (slice t-32-32 0 32 16 32)
  )
  0)"
.parse::<Pattern<_>>()
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"(elementwise-add
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   (slice v-32 0 16)
   (slice t-32-32 0 16 0 32)
  )
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   (slice v-32 16 32)
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"(concat
  (bsg-systolic-array 32 16
   v-32
   (slice t-32-32 0 32 0 16)
  )
  (elementwise-add
   (bsg-systolic-array 16 16
    (slice v-32 0 16)
    (slice t-32-32 0 16 16 32)
   )
   (bsg-systolic-array 16 16
    (slice v-32 16 32)
    (slice t-32-32 16 32 16 32)
   )
  )
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  - How do we pull a “compiler” out of an egraph?
  - How to implement a complex, multi-objective extraction process?
  - How to represent hardware sharing?





PLSE

sampl

sampa

PAUL G. ALLEN SCHOOL

W

Thank you!

https://github.com/gussmith23/glenside

https://justg.us